VNA Based Load Pull Harmonic Measurement De-embedding Dedicated to Waveform Engineering

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Abstract. This paper presents a simple methodology to observe the RF waveforms at the drain source current reference plane of the transistor, without using a complete nonlinear model. The aim is to allow Power Amplifier designers starting their work using VNA based harmonic and time domain load pull measurements, and S parameter measurements. The later measurements will be used to extract a linear model first. Then the parameters of the linear model will be used to deembed the load pull measurements directly at the voltage controlled current source plane, in order to enable waveform engineering. Because of the well know theoretic conditions that enable optimum efficiency, this methodology can also be used to avoid time consuming multi-harmonic load pull measurements. Harmonic impedances can be defined accordingly to the knowledge of the operating class addressed, while load pull optimization can be addressed to refine the fundamental matching only.

***Index Terms* — High Efficiency Power Amplifier, Class F, inverse Class F, waveform engineering, linear deembedding, Load Pull, RF load lines.**

I. Introduction

RF power amplifiers play an important role in the overall power consumption and power dissipation of base stations. It is therefore important that those amplifiers have the highest possible intrinsic efficiency. High efficiency amplifier design can be made according to several concepts, such as linear amplification with nonlinear component (LINC), [1], envelope elimination and restoration (EER) [2-3] delta–sigma modulation-based transmitters [4-5], Doherty amplifiers [6-8], Outphasing amplifiers [9-11] or Envelop tracking amplifiers [12-14].

Behind all these concepts, the main idea is to use the power transistor, which is the core component of these amplifiers, at the maximum efficiency, which correspond to the conditions where the transistor is driven in the saturated area.

In order to reduce the power consumption at high power level, one of the key is to avoid simultaneous voltage and current consumption at the transistor level. At RF and microwave frequencies, such conditions can be achieved using current and voltage waveform shaping at the drain level. Thanks to the understanding waveform shaping, designers have now widely adopted Power Amplifier (PA) design methodologies which employ high efficiency class of operating conditions, such as Class F or inverse Class F amplifiers [15-18].

For class F conditions, at the voltage controlled current source reference plane of the transistor, the waveform shaping is obtained by providing a short-circuit at the even harmonic frequencies (2nf0) while an open-circuit is provided at the odd harmonics (3nf0). For such conditions, a square-voltage waveform will be obtained while the drain current waveform will be shaped as a half-sine. Looking at the ideal RF load line, as shown on figure 1, it can be observed that simultaneous voltage and current consumptions are avoided, thus annulling the average power consumption at high power level, so a theoretic efficiency of 100% can be achieved.

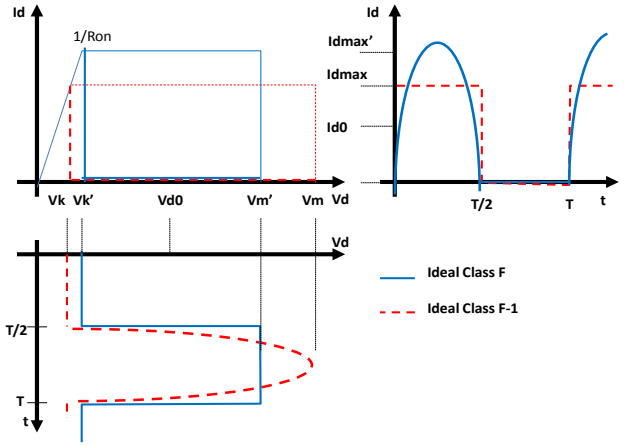

Fig. 1. Class-F and Inverse Class-F ideal waveforms

Inverse Class F concept is using the same approach. In this case, the RF waveform shaping is obtained by providing an open circuit at the even harmonic frequencies (2nf0) while a short circuit is provided at the odd harmonics (3nf0). As a result, the drain current will appear as square waveform while the drain voltage will be shaped as a half-sine. Inverse Class F provides lower peak drain current and higher peak voltage, which is preferable if a significant Dynamic On resistance of the transistor tends to reduce the available efficiency [19]. In these conditions, attention must be paid to the peak drain voltage that can reach the breakdown area. These two classes can be advantageously combined when designing a two-stage amplifier in order to take benefit from the voltage waveform shaping given by the driver for the power amplifier stage [20].

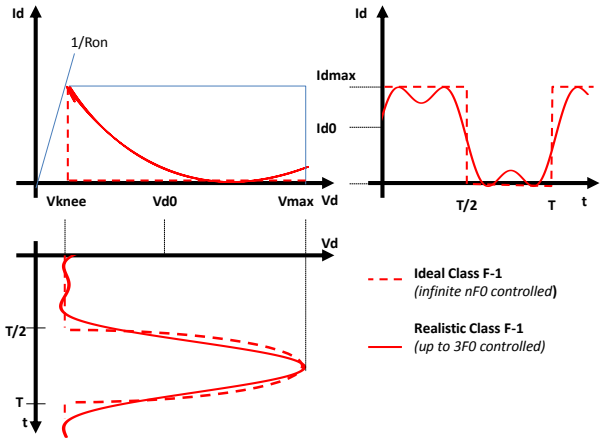

Fig. 2. Ideal and realistic Inverse Class-F wavefoms.

Using L/4 impedance transformers that convert open-circuit to short-circuit or inversely, at the different harmonics, high efficiency amplifiers can be easily designed in theory.
Nevertheless, even if well-established theory provides the optimal loading conditions, practical PA implementations are often empirical in nature.
In practice, when measuring a transistor in order to find the best efficiency, empirical optimization of harmonic load impedances using a load pull measurement systems is still the main trend [21-22]. As stated in [23], one of the most significant barriers to large-scale adoption of waveform shaping in comparison of empirical optimization is the lack of first-pass design methodology.
The main reason why the empirical approach is still used is because waveform engineering requires observing and controlling the waveforms at the intrinsic reference plane of the transistor, that is to say at the voltage controlled current source level, which is not straightforward, unless a complete and open compact electrothermal nonlinear model is extracted for the simulation [24]. Indeed the intrinsic and extrinsic parasitic elements hide the useful information that can be used to optimize the RF waveforms. In practice, the optimum loads found at the extrinsic planes do not correspond to the theoretic harmonic open and short circuits that would correspond to Class F or inverse Class F conditions [25].

II. Measurement Setup

RF time domain VNA based harmonic load pull benches are now democratized, and allows visualizing the RF waveforms at the extrinsic planes, that is to say at the calibration reference planes, using absolute magnitude and phase calibrations [26-29]. Nevertheless, because of the need for a complete an open nonlinear model to deembed the data at the current reference plane, measuring the waveforms at RF frequencies at the extrinsic reference plane is up to now more a nice-to-have feature rather than a must-to-have solution. Without an accurate model, even with on-wafer measurements, it is hard to say if Class F or inverse class F conditions are addressed.

This work therefore aims to present a method that use harmonic load pull measurements that record measured fundamental and harmonic power waves at the input and the output of the DUT. The absolute calibration in phase between the fundamental and harmonic tones is made using a phase calibrated comb generators [29]. Such a comb generator is needed because the narrow bandwidth VNA measurement systems loose the phase relationships when the Local Oscillator (LO) is frequency shifted from the fundamental tones to the harmonic tones. As depicted on figure 3, one comb generator is used to calibrate the absolute phase at the measurement plane. During the load pull measurements, four receivers are used to measure input and output a and b waves at the different tones, while the fifth receiver of the VNA which is permanently plugged to the second comb generator serves as a phase reference once the OL has been shifted.

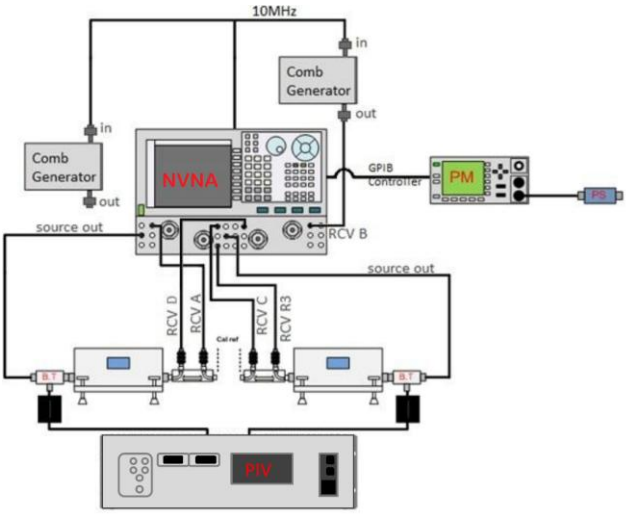

Fig. 3. Time domain VNA Based Load Pull Harmonic Measurement system

The tuners used are harmonic tuners [30], the third harmonic is driven by and active load coming from the second source of the VNA. This setup stores directly the incident and reflected power waves calibrated at the different harmonic tones. The software which controls this setup [31] enables to calculate any combination of these power waves, and to display the RF waveforms versus different power levels and impedances directly at the extrinsic planes.
De-embedding these power waves into the source current plane of the transistor is more complex than de-embedding some basic S parameter measurement using a set of two-ports S parameter bloc files, because a transistor is essential a three port device, and because the extrinsic parasitic elements cannot be measured directly. Nevertheless, thanks to the methodology proposed here, the aim is to de-embed these measurements easily, just using basic S parameter measurements previously made on the same transistor.

II. Basic Modeling Step

In order to de-embed these measured RF waveforms, a preliminary step is needed to extract the extrinsic elements. Basic S parameter measurements will be used with some explicit equations, and a final optimization [32].
The linear model extraction process uses S-Parameters to determine the transistor's extrinsic parasitic elements (Rg, Lg, Cpg, Rd, Ld, Cpd, Rs and Ls) as sketched in figure 4.

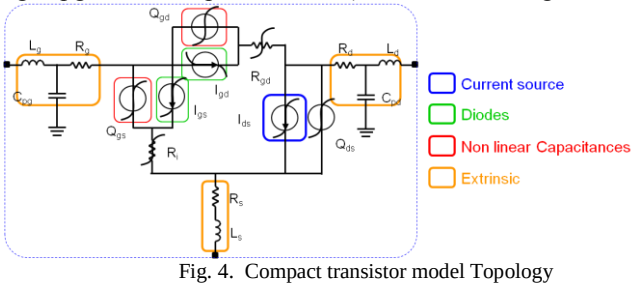

Fig. 4. Compact transistor model Topology

In open channel conditions, Cold FET S parameter measurements are made for a cold quiescent bias point (Vgs=open & Vds=0V). These S parameters are converted into Z parameters [33] to enable a direct computation of the parasitic extrinsic resistance and inductances [34-35].

$$Rs = real(Z21) - Rc/2 \quad (1)$$
$$Rd = real(Z22) - real(Z21) - Rc/2 \quad (2)$$
$$Rg\sim = real(Z11) - real(Z21) + Rc/6 \quad (3)$$
$$Ls = Im(Z21)/W \quad (4)$$
$$Ld = (Im(Z22) - Im(Z21))/W \quad (5)$$
$$Lg = (Im(Z11) - Im(Z21))/ \quad (6)$$

Where W is the channel width, and Rc the Channel Resistance of the transistor.

In closed channel conditions, the Cold FET S parameter measurements are made for the cold quiescent bias point (Vgs=Pinch-off & Vds=0V); in order to enable a direct computation of the parasitic extrinsic capacitances.

$$Cpd = (Im(Y22) + Im(Y21))/W \quad (7)$$
$$Cpg = (Im(Y11) + 2 * Im(Y21))/W \quad (8)$$

Where Y are the admittance parameters [33]. Even if the device is realistically biased in Cold FET mode, these operating conditions will not correspond exactly to the theoretic hypothesis that must be observed when using the equations (1-8). The intrinsic part of the transistor will never be a perfect short-circuit nor a perfect open-circuit. Nevertheless, these first equations are useful to determine the boundaries of an optimization that will refine these extrinsic values later, tanks to Hot FET S parameter measurements, when the device is biased at the nominal quiescent bias point.

Using IVCAD tool [32], the optimization process is done as follow: once an arbitrary set of extrinsic elements are defined within some boundaries fixed by the user thanks to previous Cold FET measurements, the extrinsic S-Parameter measurements can be de-embedded to the intrinsic reference plane, and a corresponding set of intrinsic parameters (Cgs, Cgd, Gm, Gd, Cds, Ri, Tau, Rgd) can be extracted using explicit equations [34-35] in order to fit the Hot FET S parameter measurements.

During this process [31], the goal of the linear modeling optimization is to determine the values for the extrinsic parameters which in turn provide a set of intrinsic parameters which have a fixed value versus frequency. Measured and calculated extrinsic or intrinsic S-Parameters are compared over the entire RF bandwidth, and the linear modeling optimization is run until a good fit is achieved. This step can be done using several S parameter measurement files measured at different Hot FET quiescent bias points in order to avoid unrealistic calculus of extrinsic and intrinsic parameters.

Once the optimization is finished, the linear model is available, and the load pull measurements can be deembedded. In the following table, as an illustration, a set of parameters describes a linear model, they will be used for the deembedding work presented in this work.

Extrinsic Parameters [R (Ω), L(H), C(F)]		**Intrinsic Parameters**	
" Rg " =	" 2.742 "	" Cgs " =	" 8.206E-13 "
" Lg " =	" 4.909E-11 "	" Cgd " =	" 7.880E-14 "
" Cpg " =	" 1.205E-13 "	" Gm " =	" 0.093 "
" Rd " =	" 4.018 "	" Gd " =	" 0.001 "
" Ld " =	" 6.396E-11 "	" Cds " =	" 6.284E-14 "
" Cpd " =	" 5.676E-14 "	" Ri " =	" 0.223"
" Rs " =	" 1.986"	" Tau " =	" 4.164E-12 s"
" Ls " =	" 5.104E-12 “	" Rgd " =	" 2.673 “

Table. 1. Linear Model parameters

II. Extrinsic to Intrinsic Deembedding

The deembedding will require an initial processing in order to transform the vector harmonic power waves a1, a2, b1, b2 measured by the load pull setup into equivalent voltage and current vectors v1ext, v2 ext, i1ext, i2 ext [36]. The extrinsic to intrinsic deembedding can now be achieved as sketched in the following figure.

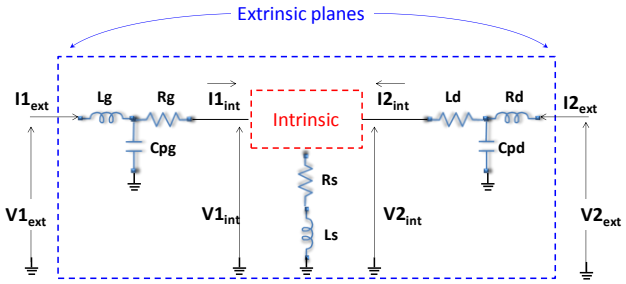

Fig. 5. Electrical Scheme used for linear deembedding

Once converted, these currents and voltages are de-embedded using the following equations:

$$V1_{int} = V1_{ext} - I1_{ext} \times Z_{Lg} - Rg \times \left(I1ext - \left(\frac{V1_{ext} - ZLg \times I1ext}{ZCpg} \right) \right) \quad (9)$$

$$V2_{int} = V2_{ext} - I2_{ext} \times Z_{Ld} - Rd \times \left(I2ext - \left(\frac{V2_{ext} - ZLd \times I2ext}{ZCpd} \right) \right) \quad (10)$$

$$I1_{int} = I1_{ext} - \left(\frac{V1_{ext} - ZLg \times I1ext}{ZCpg} \right) \quad (11)$$

$$I2_{int} = I2_{ext} - \left(\frac{V2_{ext} - ZLd \times I2ext}{ZCpd} \right) \quad (12)$$

As a consequence, the current and voltage RF waveforms are now available at the intrinsic reference planes, but these ones are not yet the ones that must be used for waveform engineering. Indeed, it is necessary to visualize these waveforms directly at the voltage controlled output current source reference plane, to get rid of the influence of the parasitic intrinsic output conductance of the transistor, (Cds).

II. Deembedding from Intrinsic to Current Source Reference Plane

Once the drain and voltage waveforms at the intrinsic reference plane have been calculated, thanks to the linear model extraction, the Rds and Cds intrinsic parameters are know.

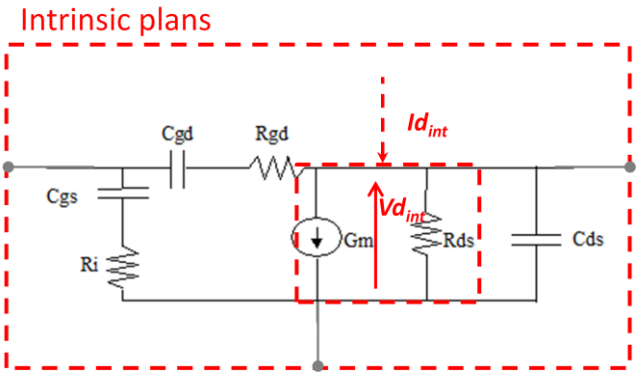

Fig.6. Electrical Schematic of the Intrinsic Model

These parameters allow deembedding the output current and voltages directly at the current source plane, using equations (13-15).

$$Vd_{int} = V2_{in} - Z_S \times (I1in + I2in) \quad (13)$$

$$Id_{int} = I2_{in} - \left(\frac{Vd_{in}}{ZCds}\right) \quad (14)$$

with

$$ZCds = \frac{1}{j\times\omega\times Cds}. \quad (15)$$

It can be noticed that waveform engineering is useful when the device is saturated in order to generate the wanted harmonic current and voltages tones, and to reach the maximum PAE area. As a matter of fact, the DUT operates in nonlinear conditions, thus, using a linear model to deembed the measurements can be questionable.

To answer such a question, it must be noted that the extrinsic parameters (Rg, Rd, Rs, Lg, Ld, Ls, Cpg and Cpd) are constant, independent of the frequency and independent of the power level. Thus a linear deembedding is valid in these conditions. Nevertheless Rd ad Rs values are linearly influenced by the Temperature increase caused by the mean power consumption at high power level. Below is an example of the extrinsic resistance variation versus T°.

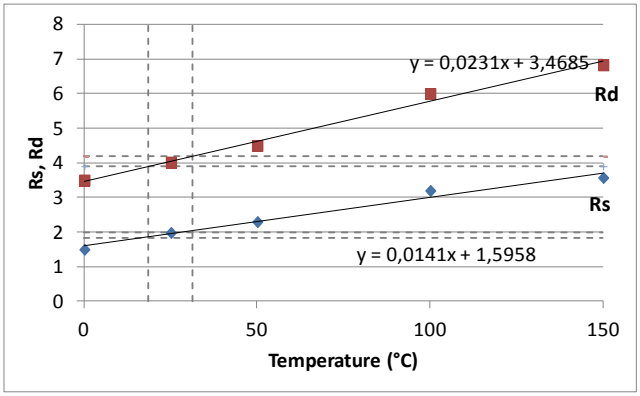

Fig. 7. Extrinsic resistance variation versus T°

In Figure 7, the extrinsic resistance variation caused by the temperature variation is strongly linked to the transistor technology and topology. In this example, the transistor had a 2mm periphery with a thermal resistance of 6,3°C/W.

As a consequence, this approach is not an absolute and formal de-embedding methodology, by rather a practical and straightforward concept. A more rigorous approach would be to extract a thermal linear model that would take into account the junction temperature of the transistor. Extracting such a model would require S parameters taken at different chuck temperatures and other electrical measurements to extract the corresponding thermal impedance, adding more complexity in the process. That would reduce the interest of the method proposed here.

In should be highlighted that when dealing with high efficiency, such as Class F or inverse Class F conditions, the power consumption variation is also reduced, as illustrated below.

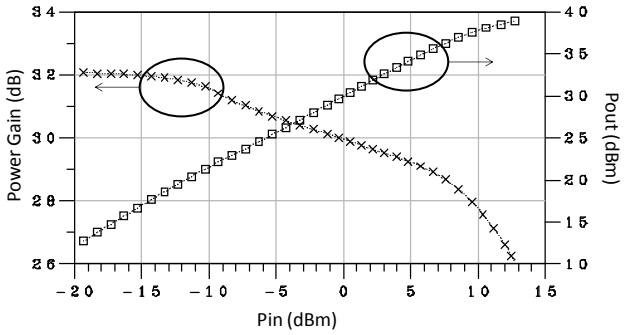

Fig. 8. Power Gain and Output Power (Class F), Vg =-1.9V, Vd = 40V, F0=1.57GHz

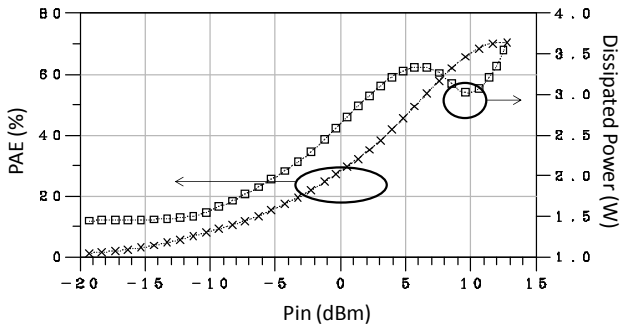

Fig. 9. PAE and Dissipated Power (Class F), Vg =-1.9V, Vd = 40V, F0=1.57GHz

In our example, this lead to a resistance variation lower than 8% over the temperature range as shown by the dashed lines of figure 7, making the concept valid to deembed the RF waveforms. The same conclusion can be used for Cds and Rds.

Another question that may appear could be linked to the fact the output capacitance Cds is supposed to be linear. Indeed, in [37], some investigations of a Class F-1 power amplifier using a nonlinear output capacitor model have been made. It has been shown that the nonlinear output capacitance can be used during the simulation to generate higher magnitude of the voltage at the second harmonic, thus increasing a bit the prediction of the maximum efficiency achievable. Nevertheless, is it generally observed that the output capacitance and resistance are

weakly nonlinear, and they can be described by a linear model.

II. Observing the RF Waveforms

Once these two deembedding steps are achieved, the RF waveforms can be observed at both extrinsic and courant source reference planes. As an illustration, some waveforms obtained for class F conditions are provided using the linear model provided in Table 1.

A first load pull optimization has been done in order to determine the optimal fundamental load impedance for maximum efficiency, with the fundamental source impedance matched to the conjugate value of the transistor input impedance measured in linear conditions. Harmonic impedances where tuned to 50Ω. Then, the harmonic load impedances where tuned directly to their theoretic values in order to reach the Class F conditions at the source current plane. (Zload_int_2f0=Short, Zload_int_3f0=Open). The power performances measured are displayed on figures 8 & 9.

The RF waveforms measured are in-line with the shapes that were expected, taking into account the fact the measurements were limited to the third harmonic.

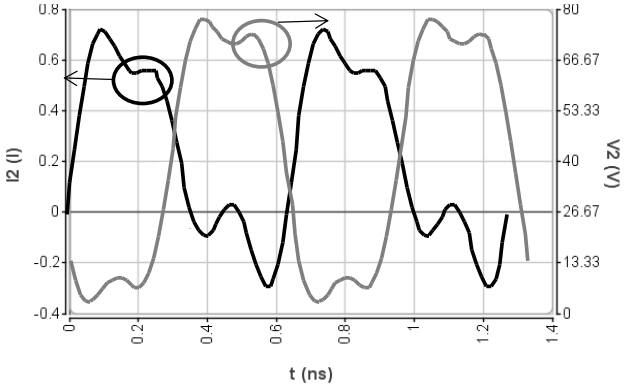

Fig. 10. RF Waveform measurement in the extrinsic planes

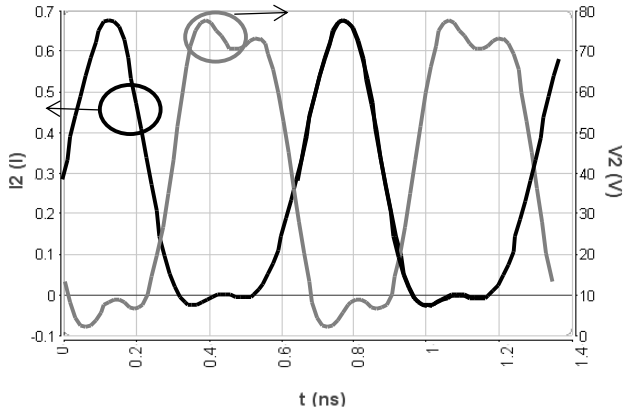

Fig. 11. RF Waveform measurement in the Current Source plane

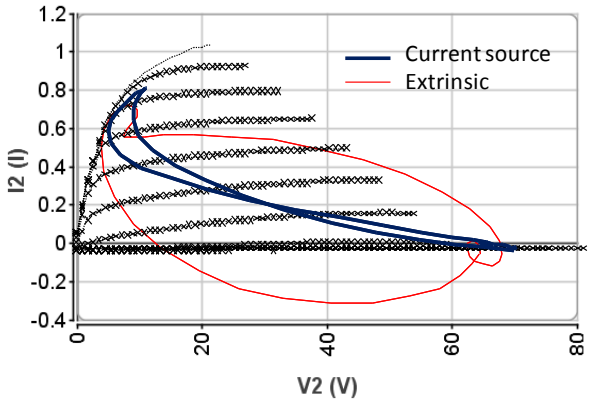

Fig. 1. RF Load lines

Looking at the output voltage waveform, it can be observed that the swing of the extrinsic voltage is reduced in magnitude, mainly because of the extrinsic resistances which create a voltage drop. In addition, the parallel capacitances and serial inductances generate a negative output current, which is not the case when looking directly at the current source plane. Both phenomena can be observed simultaneously when plotting the RF load lines, highlighting the fact that Waveform engineering cannot be used at the extrinsic reference plane directly when performing time domain load pull measurements.

IV. Conclusion

A deembedding methodology has been proposed in order to observe the load pull waveform measurements at the current source reference plane of a transistor. The aim is to allow waveform engineering to design high efficiency amplifiers, even without using a complete nonlinear electro-thermal model. The nonlinear characteristics and optimal impedance matching are directly provided by the multi-harmonic load pull measurement setup, while the deembedding parameters are provided a linear model extracted from S parameter measurements.

Using these tools, a deeper understanding of the operating class used for high efficiency can be achieved.

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