High Efficiency Doherty Power Amplifier Design using Enhanced Poly-Harmonic Distortion Model

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Abstract. This paper presents new identification methodologies dedicated to packaged transistor behavioral modeling. Using the background of the Poly-Harmonic Distortion (PHD) model formalism, the extension of the model kernels description up to the third order makes the behavioral model more robust and accurate for a wide range of impedance loading conditions, which is a primordial when designing a High Power Added Efficiency Doherty Amplifier, where a load impedance variation can be observed as a function of the power level. In this paper, a model of a 15 W GaN Packaged Transistor has been extracted from Load Pull measurements for Class AB and Class C conditions. This new Enhanced PHD model (EPHD) and the original PHD model are benchmarked against Load Pull measurements in order to check the new formulation. An advanced validation at the circuit level was done in order to verify the ability of the EPHD model to predict the overall Doherty Amplifier performances.

***Index Terms* — High Efficiency, Doherty PA design, Packaged Transistors, Poly Harmonic Distortion, Behavioral Modeling, Load Pull**

I. INTRODUCTION

Doherty theory is now well known [1][2][3][4] and this topology is suitable for the design of High Power Added Efficiency power amplifiers. Doherty Power Amplifier (DPA) principle is based on a Load impedance modulation linked to the power level at the input of both main and auxiliary amplifier branches.

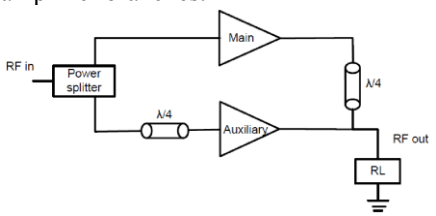

Fig. 1. Doherty PA principle

The main branch is usually made of a transistor driven in Class AB, while the auxiliary branch is made of a transistor used in Class C. At low power level, when the auxiliary transistor is off, the overall efficiency is given by the efficiency of the main branch. When the input power increases, the gain of the auxiliary transistor rises, and it introduces a modulation of the loading conditions for the main transistor, modifying the overall efficiency. This modulation is due to the asymmetrical combination of powers between these two branches. If this modulation is optimized, the efficiency of the overall amplifier can be increased over a large dynamic power range. Equation (1), provides the relationships for the Power Added Efficiency (PAE) and the Dissipated Power (Pdiss) of each branch:

$$\mathrm{PAE_{DPA}} = \frac{\mathrm{P_{diss_{main}}} * \mathrm{PAE_{main}} + \mathrm{P_{diss_{aux}}} * \mathrm{PAE_{aux}}}{\mathrm{P_{diss_{main}}} + \mathrm{P_{diss_{aux}}}} \quad (1)$$

In such a design, the transistor model must stay accurate to predict the PAE performance versus various output power levels whatever the loading impedances conditions for each transistor (Class AB & C).

Conventionally, Compact model are used due to their ability to describe the behavior of the transistor along the output back-off range for important load variations. Unfortunately, extracting a compact model of a packaged transistor is a difficult issue because the dispersive behavior of the package hides the other elements of the transistor. As explained in [5][6], the design of the matching circuit can be derived from load-pull data measured directly at the package reference planes. It gives good results in drain efficiency and output power, but nevertheless, the design has been developed using a model provided by the device manufacturer.

The method to extract a Poly-Harmonic Distortion (PHD) nonlinear behavioral model has been introduced in [7]-[8]. This approach was applied at first for 50Ω devices (amplifiers). Then this methodology has been generalized for non-50 Ω devices (transistors) [9]. In order to make the PHD model suitable for different load impedance conditions, a juxtaposition of several elementary models have been proposed, in order to provide a global table-based model.

The load interpolation capability of this global model is linked to software platform used, but this one is also linked to the grid density of the load impedances used for the model extraction. This increases significantly the measurement time needed to ensure proper model convergence. In addition, the model extraction capability is not robust.

Some recent works tried to increase the model flexibility and robustness of the model against different loading conditions [10] with higher order of distortion terms. The results of this method are very good and linked to optimized measurement process ensure minimum load pull measurements necessary for a proper high order model extraction.

In this paper, a third order power expansion of the PHD kernels is proposed in order to take into account the nonlinear influence of the load impedance variations, while keeping a straightforward model extraction methodology. The assumption made in this work relies on the hypothesis that the non linear influence of output port incident wave is observed only at fundamental frequency (harmonic influences are linear). This assumption limits strongly the model complexity and allows extraction process from any NVNA measurement set up without any optimization process.

This approach provides some good results for the prediction of the main transistor behavior, but also for the auxiliary transistor, even in case of low isolation between the two branches.

II. ENHANCED PHD MODEL

A. Formalism

On Figure 2 a nonlinear device is sketched, with the respective incident and scattered waves ai(t), bi(t) which correspond to the incident and reflected power waves on port numbers i =1,2.

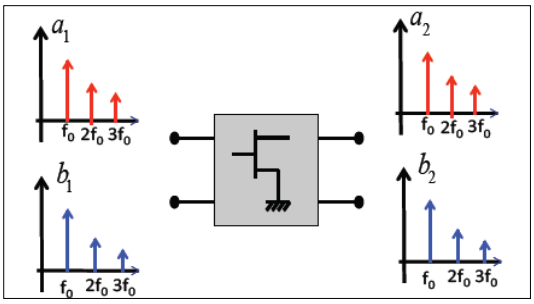

Fig. 2. Harmonic superposition principle

The output wave bi(t) can be expressed as a sum of fundamental and harmonic modulated tones (1):

$$b_i(t) = \mathrm{Re}\left\{\sum_{k=0}^{N} \tilde{b}_{ik}(t) e^{j2\pi k f_0 t}\right\} \quad (2)$$

The general equation of a nonlinear system maps the entire set of incident waves in envelope domain as (2).

$$\tilde{b}_{ik}(t) = f_{NL}\begin{pmatrix} \tilde{a}_{11}(t), \tilde{a}_{12}(t), \tilde{a}_{13}(t), \ldots \\ \tilde{a}_{21}(t), \tilde{a}_{22}(t), \tilde{a}_{23}(t), \ldots \\ \tilde{a}^*_{11}(t), \tilde{a}^*_{12}(t), \tilde{a}^*_{13}(t), \ldots \\ \tilde{a}^*_{21}(t), \tilde{a}^*_{22}(t), \tilde{a}^*_{23}(t), \ldots \end{pmatrix} \quad (3)$$

Assuming that the main nonlinearity is driven by the incident power wave $a_{11}(t)$ at the fundamental frequency given at the input port, harmonic superposition can be applied to (2), resulting in a relationship governing two-port nonlinear systems:

$$\tilde{b}_{ik}(t) = \sum_{jl} S_{ik,jl}\left(|\tilde{a}_{11}(t)|\right) P^{k-l} \tilde{a}_{jl}(t) + \sum_{jl} T_{ik,jl}\left(|\tilde{a}_{11}(t)|\right) P^{k+l} \tilde{a}^*_{jl}(t) \quad (4)$$

with $P = e^{j\varphi_{\tilde{a}_{11}}(t)}$

Equation (3) is the general formulation of the PHD model. This expression is by nature limited to first order expansion. In other words, this truncature assumes that the behavior of the device is linearly dependant of the power waves $\tilde{a}_{jl}(t)$ when $j,l \neq 1,1$. This hypothesis is true when the device is driven under low mismatch conditions against the reference impedance (realistic for amplifier model). In case of highly mismatched conditions, it is necessary to extend the nonlinear description of equation (2) in order to model the influence of the a_{21} on b_{ik} power waves.

$$\begin{aligned}
&\tilde{b}_{ik}(t) = S_{ik,11,1}\left(|\tilde{a}_{11}(t)|\right)\tilde{a}_{11}(t) + S_{ik,21,1}\left(|\tilde{a}_{11}(t)|\right)\tilde{a}_{21}(t) \\
&+T_{ik,21,1}\left(|\tilde{a}_{11}(t)|\right)P^{k+1}\tilde{a}^*_{21}(t) \\
&\text{--- order1} \\
&+S_{ik,21,2}\left(|\tilde{a}_{11}(t)|\right).P^{-1}.\tilde{a}^2_{21}(t) + T_{ik,21,2}\left(|\tilde{a}_{11}(t)|\right).P.\,\tilde{a}_{21}(t).\tilde{a}^*_{21}(t) \\
&+U_{ik,21,2}\left(|\tilde{a}_{11}(t)|\right)P^3.\tilde{a}^*_{21}(t)^2 \qquad (5) \\
&\text{--- order2} \\
&+S_{ik,21,3}\left(|\tilde{a}_{11}(t)|\right).P^{-2}.\tilde{a}^3_{21}(t) + T_{ik,21,3}\left(|\tilde{a}_{11}(t)|\right).\,\tilde{a}_{21}(t)^2.\tilde{a}^*_{21}(t) \\
&+U_{ik,21,2}\left(|\tilde{a}_{11}(t)|\right)P^2.\tilde{a}_{21}(t).\tilde{a}^*_{21}(t)^2 + \; + W_{ik,21,3}\left(|\tilde{a}_{11}(t)|\right)P^4.\tilde{a}^*_{21}(t)^3 \\
&\text{--- order3} \\
&+\ldots\ldots \\
&\textit{with } P = e^{j\varphi_{\tilde{a}_{11}}(t)}
\end{aligned}$$

In order to keep a reasonable complexity, the nonlinear expansion of the model kernels will be limited to a third order.

B. Kernels extraction

In order to illustrate the extraction methodology, a complete model extraction is described, while taking into account two harmonics (f0 and 2f0). The first step is run to measure the non-linear state due to the incident wave a_{11} at f0. For the reference load impedances at f0 and 2f0, the equation to be solved for each level of input power is described in equation (6),

$$S_{ik,11} = \left[a_{11}\right]^{-1} \times \left[b_{ik}\right] \quad (6)$$

Generally, on the Smith Chart, the reference impedances are chosen close to the center of the area of interest. In a second step, the influences of the incident wave on the output port at f0 (a_{21}) are measured individually for a set of load impedances along a large pattern of impedances, the harmonic impedance at 2f0 is kept unchanged (on the reference). As depicted on equation (7), a matrix calculation by LSQR is solved for each injected power level.

$$\begin{bmatrix} S_{ik,21} \\ T_{ik,21} \\ S_{ik,21,2} \\ T_{ik,21,2} \\ U_{ik,21,2} \\ S_{ik,21,3} \\ T_{ik,21,3} \\ U_{ik,21,3} \\ W_{ik,21,3} \end{bmatrix} = \begin{bmatrix} \tilde{a}_{210} & \tilde{a}^*_{210} & \tilde{a}^2_{210} & \ldots. & \tilde{a}_{210}.\tilde{a}^{*2}_{210} & \tilde{a}^{*3}_{210} \\ \ldots & & & & & \\ \ldots & & & & & \\ \ldots & & & & & \\ & & & & & \\ & & & & & \\ & & & & & \\ & & & & & \\ \tilde{a}_{21m} & \tilde{a}^*_{21m} & \tilde{a}^2_{21m} & \ldots\, \tilde{a}_{21m}.\tilde{a}^{*2}_{21m} & \tilde{a}^{*3}_{21m} \end{bmatrix}^{-1} \times \begin{bmatrix} \tilde{b}_{ik,0} \\ \ldots \\ \ldots \\ \\ \\ \\ \\ \\ \tilde{b}_{ik,m} \end{bmatrix} \quad (7)$$

The P terms are equal to zero and the index m+1 is the total number of impedances for the pattern defined at f0. Then, the influence of each incident wave (a1 at 2f0 ; a2 at 2f0) on each reflected wave (b1 and b2 at f0 and 2f0) are measured, one by one. Each system is solved by the matrix calculation depicted in (8) for n impedances pattern.

$$\begin{bmatrix} S_{ik,jl} \\ T_{ik,jl} \end{bmatrix} = \begin{bmatrix} \tilde{a}_{jl0} & \tilde{a}^{*}_{jl0} \\ \cdots & \\ \cdots & \\ \tilde{a}_{jln} & \tilde{a}^{*}_{jln} \end{bmatrix}^{-1} \times \begin{bmatrix} \tilde{b}_{ik,0} \\ \cdots \\ \cdots \\ \tilde{b}_{ik,n} \end{bmatrix} \quad (8)$$

When these steps are finished, the model is extracted.

Finally, the previous method is applied for several frequencies and it enables the capture of the frequency dispersion of the models kernels.

III. MODEL RESULTS

A. AB Class Transistor Models extraction and validation

The first GaN model extraction is done for Class AB conditions. In order to get a fair benchmark, both PHD and EPHD models were extracted within the same area of impedances, and with a similar grid density (49 impedances at f0 and 6 impedances @2f0 and 3f0).

Fig. 3. Extraction data PHD (blue) versus EPHD (purple).

This area of impedance was preliminary identified thanks to preliminary load pull measurements in order to find optimal PAE area. Over the dynamic range used, the measurement time needed to extract the PHD model using a tickle tone is about 15 min per impedance, while the time needed for the EPHD extraction (without tickle tone) is 30 seconds per impedance. Thanks to IVCAD software platform, the EPHD is directly extracted from the load pull data without any optimization procedure. The load harmonic pull measurements must be done with an absolute harmonic phase calibration, using a comb generator [11]

The two models are then benchmarked, against additional load pull measurements which have not been directly used for the model extraction. Interpolation and extrapolation capabilities of each model will be evaluated.

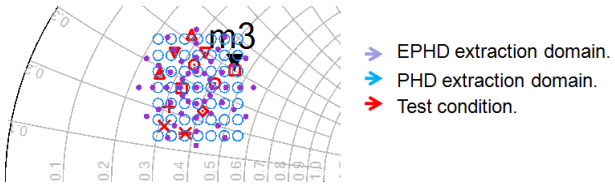

Fig. 4. Interpolation conditions (red impedances).

For Class AB conditions, as sketched in figure 5 and 6, both PHD and EPHD models provide a good fit against the measurement results. Nevertheless a superior accuracy for the EPHD model can be noticed.

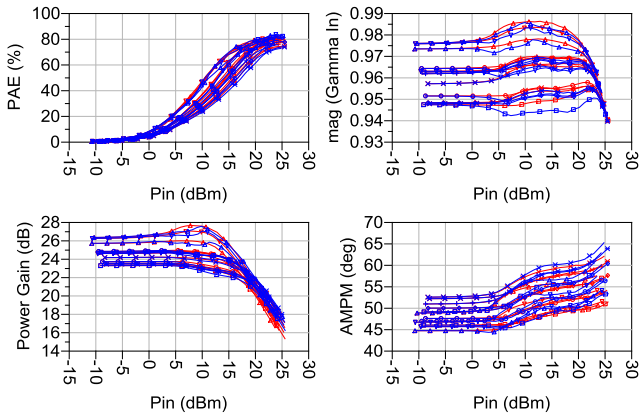

Fig. 5. PHD interpolation results (blue) versus Measurements (red).

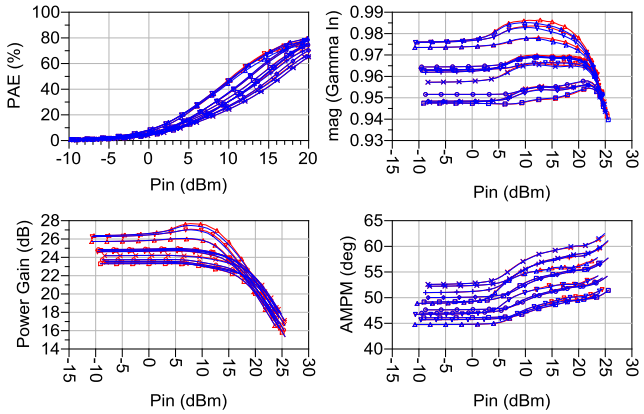

Fig. 6. EPHD interpolation results (blue) versus Measurements (red).

A second test is done under extrapolation conditions:

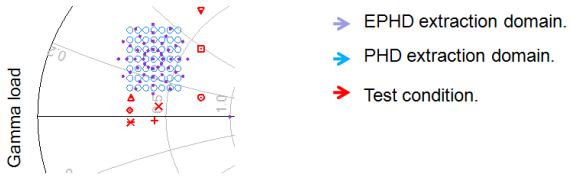

Fig. 7. Extrapolation conditions (red impedances).

For Class AB conditions, the results provided by the PHD model in extrapolation mode are shown in the following figure:

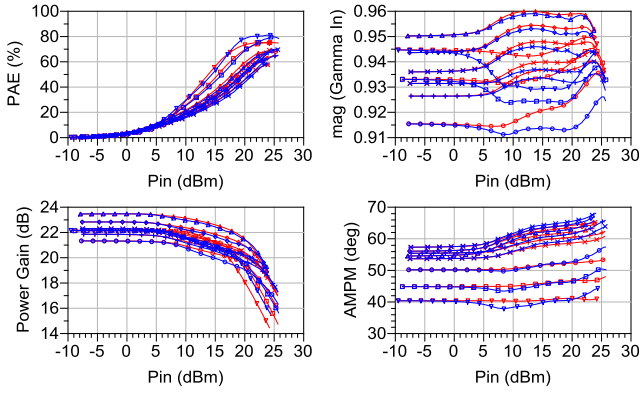

Fig. 8. PHD extrapolation results (blue) versus Measurements (red).

In the worst conditions with the set of extrapolated impedances used, the PHD model leads to some inaccuracies

for the PAE estimation (7points optimistic), as for the Power Gain (up to 1.2 dB).

The same process will be applied to the EPHD evaluation:

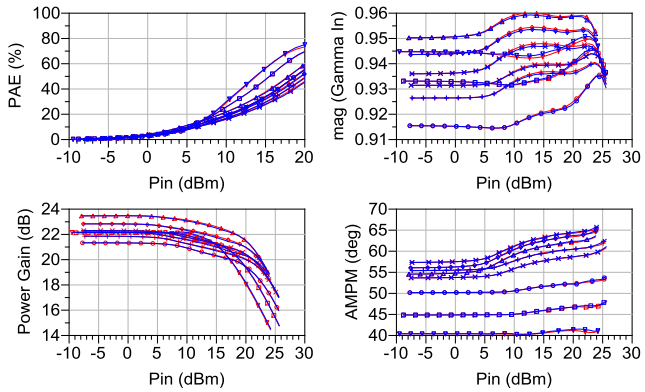

Fig. 9. EPHD extrapolation results (blue) versus Measurements (red).

It can be observed that the EPHD model provides a very good agreement with the measurements, even for extrapolation conditions. This is of prime importance for the design the Doherty where the load impedance of the Class AB branch can be modulated versus power level. The same process was carried out with the Class C conditions, with the same conclusion as depicted in the following illustration:

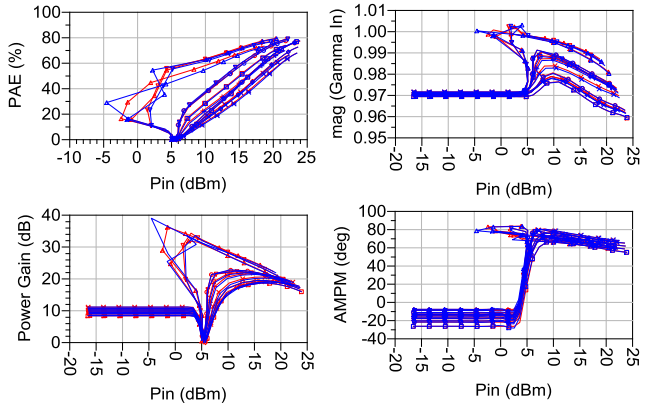

Fig. 10. EPHD interpolation results (blue) versus Measurements (red) for C-Class conditions

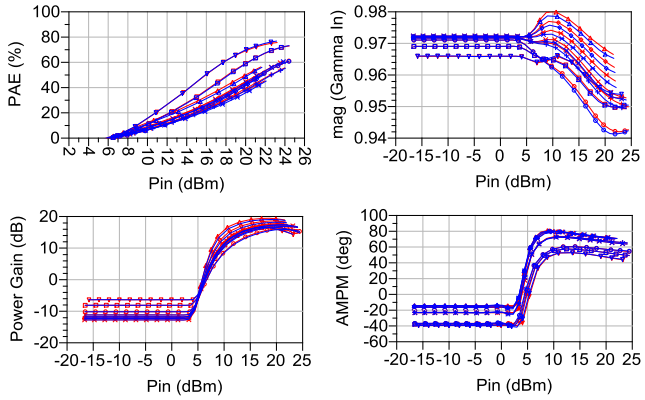

Fig. 11. EPHD extrapolation results (blue) versus Measurements (red) for C-Class conditions

In the following section, an additional step of validation is carried out. This one is done at the circuit level, in order to evaluate the ability of each model to predict the overall Doherty Design performances. Both PHD and EPHD models were used in Class AB and Class C conditions, while the load impedance is modulated against the power level.

B. Doherty simulation

In the following figure, the general performances of the Doherty design are simulated in the ADS software from Keysight, using both models. The performances are then compared with the measurement results.

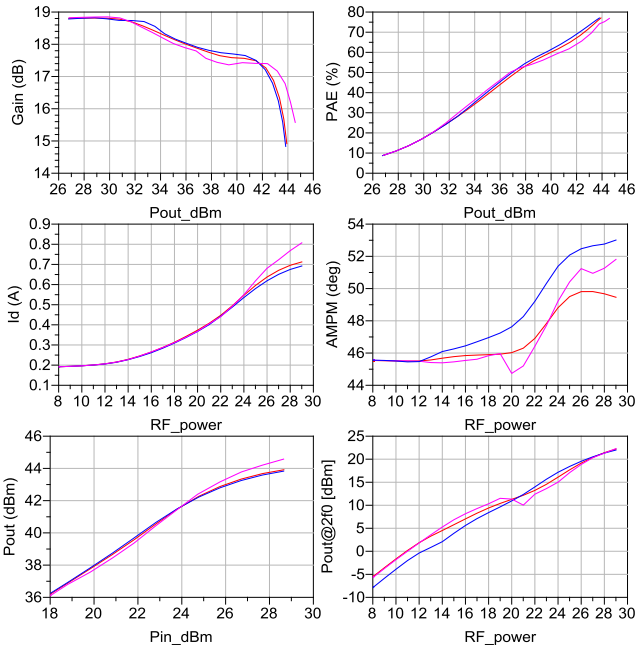

Fig. 12. EPHD simulation results (blue) versus PHD simulation results (pink) and Reference results (red)

The Doherty PA measurements and the EPHD model prediction leads to quasi-identical results in term of Power, Gain and PAE. The PHD model provides some differences which can be quantified in the figure 8.

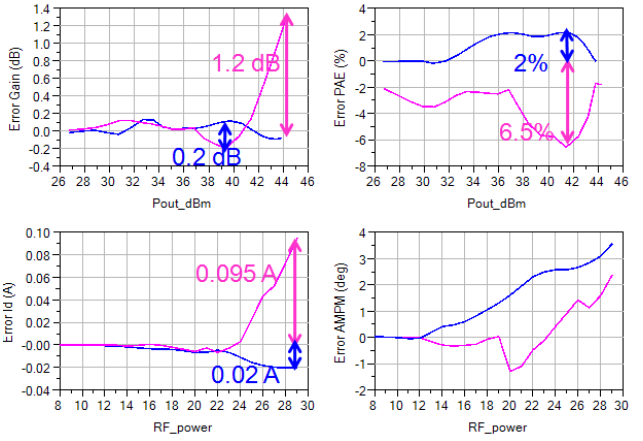

Fig. 13. Global errors EPHD simulation results (blue) and PHD (pink).

In this work, the differences between the simulation and the measurements given by the PHD model use can reach an error of 6.8 points for the PAE estimation, and 1.2 dB for the Gain, while the EPHD model decrease these errors respectively to 2 points and 0.2dB.

Note: some convergence issues can be also observed because of the insufficient isolation between the two branches. While the modulation of the load impedance for the class AB transistor is wanted, the modulation of the load impedance for the C class transistor cannot be avoided. It has been observed that this phenomenon can cause some convergence issues. As an illustration, Fig 9 highlights the variation of the load impedance of both Class AB and Class C branches.

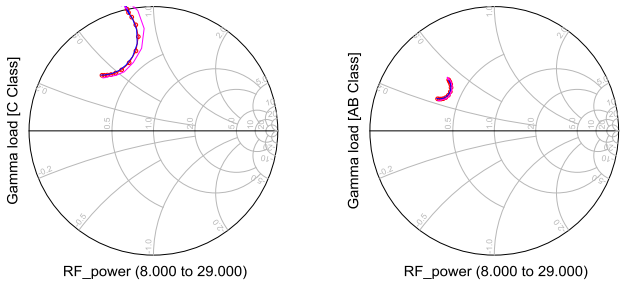

Fig. 14. Prediction on the gamma load trajectory EPHD (blue) in-situ measurements (red square) and PHD (pink)

In these conditions, the robustness of the model for extrapolation is very useful to avoid some simulation discrepancies.

IV. Conclusion

The ability of the EPHD model to reproduce the good behavior of packaged transistors in a design flow dedicated to Doherty power amplifier have been proved, with a maximum error of 2 points regarding the PAE, and about 0.2dB in output power. In addition with the time saved to extract the model during the load pull measurements, another benefit of such method is the simplification of the model extraction. The model is directly extracted from VNA based Load Pull measurement without any tuning, without any optimizations.

IV. Acknowledgments

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