Noisecom

Noise on Vcc Webinar

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Webinar Agenda

- Noise on Vcc
- Major sources of IC chip interference
- Susceptible Device Types
- Example PLL circuit
  - Basic PLL circuit description
  - Noise effects the VCO
  - Example Test System
- JV9000 – Noise on Vcc test system
- Noise effect on timer example and Vcc Test Set Up

What is Noise on Vcc?

- Extraneous voltage in the signal or supply paths
- It can be large enough to affect the integrity of operations of digital devices
- Causes:
  - Digital high speed switching outputs
  - Vcc droop and ground bounce
  - SMPS (Switch-mode power supply) noise
  - EMI/cross-talk

Why Testing Noise on Vcc is important?

- Need to ensure immunity against noise

  Designers and manufacturers of integrated circuits and small dense PCBs need to ensure their products offer sufficient immunity against Vcc noise and other jitter.

- High frequency noise can disturb IC functionality

  While Vcc specifications of integrated circuits define the operational range of the device, high frequency noise coupled on Vcc can disturb their functionality even when it is operating within the specified Vcc limits.

- Shunt capacitors may not be sufficient

  Placing a shunt capacitor adjacent to the VCC pin may no longer be sufficient.

- Lower rail voltages exasperates the problem

  Noise on the rail that was once negligible has now become intolerable in modern devices partly due to ever dropping rail voltages (sometimes below 1V). Lower Vcc voltages translates into narrower eye diagrams that easily close with the presence of noise.

- Improve noise immunity by design

  Ability to real-time test response to noise allows for design improvements to improve noise immunity

Impacts of Noise on IC Supply Voltage

Noise on supply has direct implications on performance and robustness of analog, digital, mixed signal and RF ICs

- Digital ICs:

  Broadband or discrete frequency noise on the Vcc supply can introduce jitter on high speed data lines and degrade system performance

- Analog/RF ICs:

  Noise on the supply could couple into the analog output degrading SNR or SINAD of the signal therefore degrade system performance.

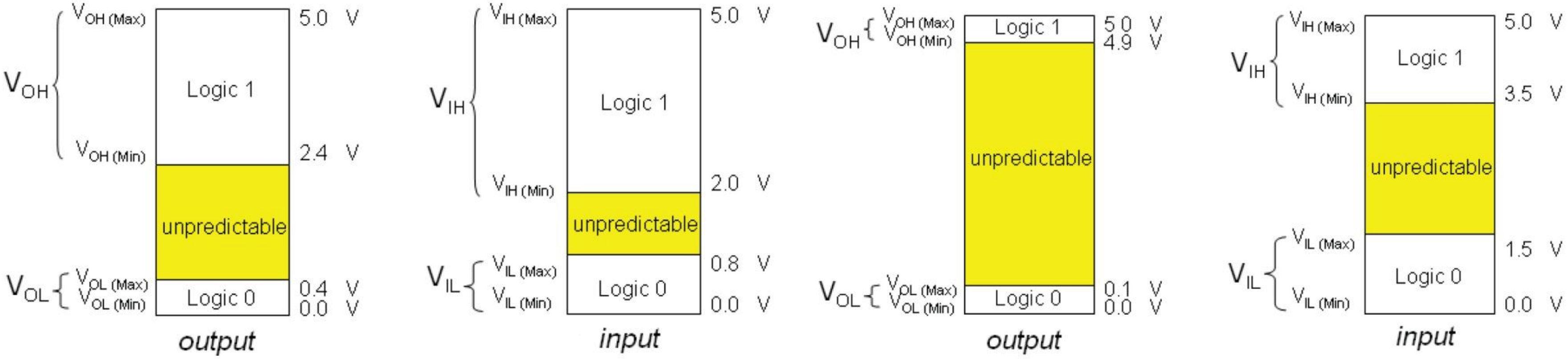
- Mixed Signal ICs:

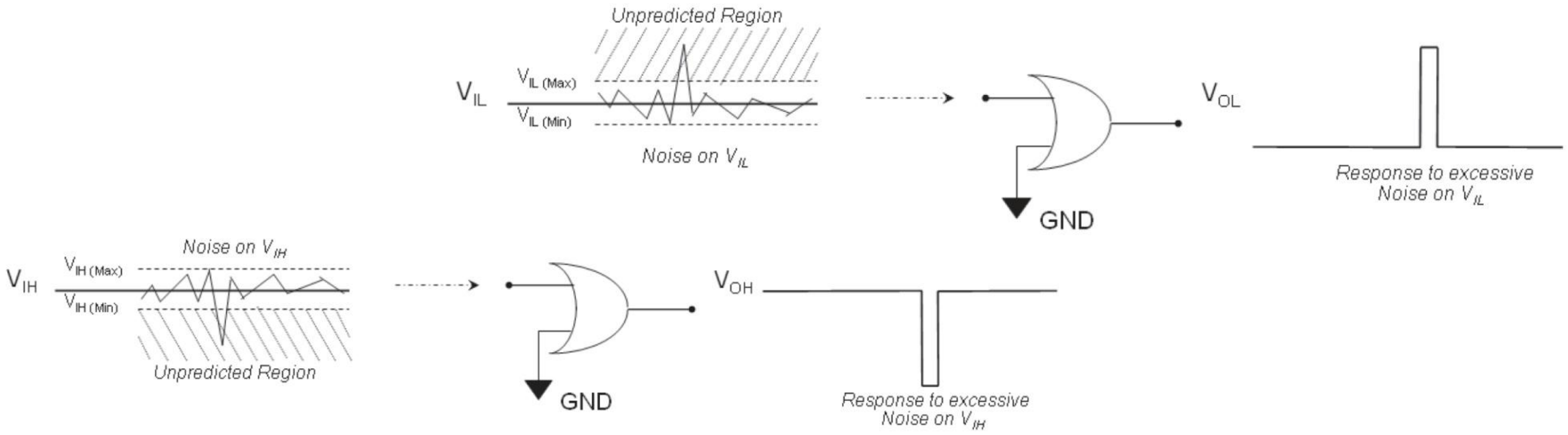
  Both effects can be observed depending on the type of ICs. (i.e. DAC, ADC,..etc)

Noise Immunity

TTL

CMOS





Noise Immunity

VNH = VOH (Min) - VIH (Min)
VNL = VIL (Max) - VOL (Max)

Noise margins for TTL and CMOS using the above:

TTL :

VIH(Min) = 2.0 V, VIL(Max) = 0.8 V,
VOH(Min) = 2.4 V, VOL(Max) = 0.4 V
VNH = VOH (Min) - VIH (Min) = 2.4 V – 2.0 V = **0.4 V**
VNL = VIL (Max) - VOL (Max) = 0.8 V – 0.4 V = **0.4 V**

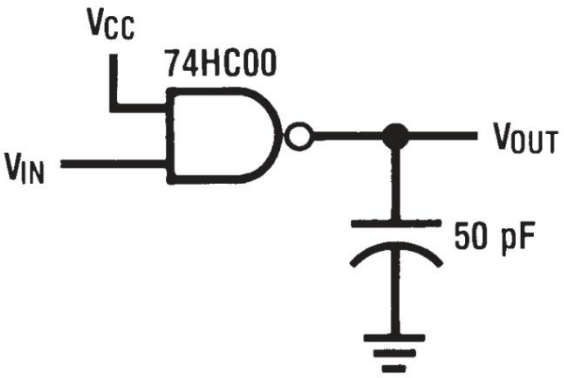
CMOS :

VIH(Min) = 3.5 V, VIL(Max) = 1.5 V,
VOH(Min) = 4.9 V, VOL(Max) = 0.1 V
VNH = VOH (Min) - VIH (Min) = 4.9 V – 3.5 V = **1.4 V**
VNL = VIL (Max) - VOL (Max) = 1.5 V – 0.1 V = **1.4 V**

1.8V CMOS:

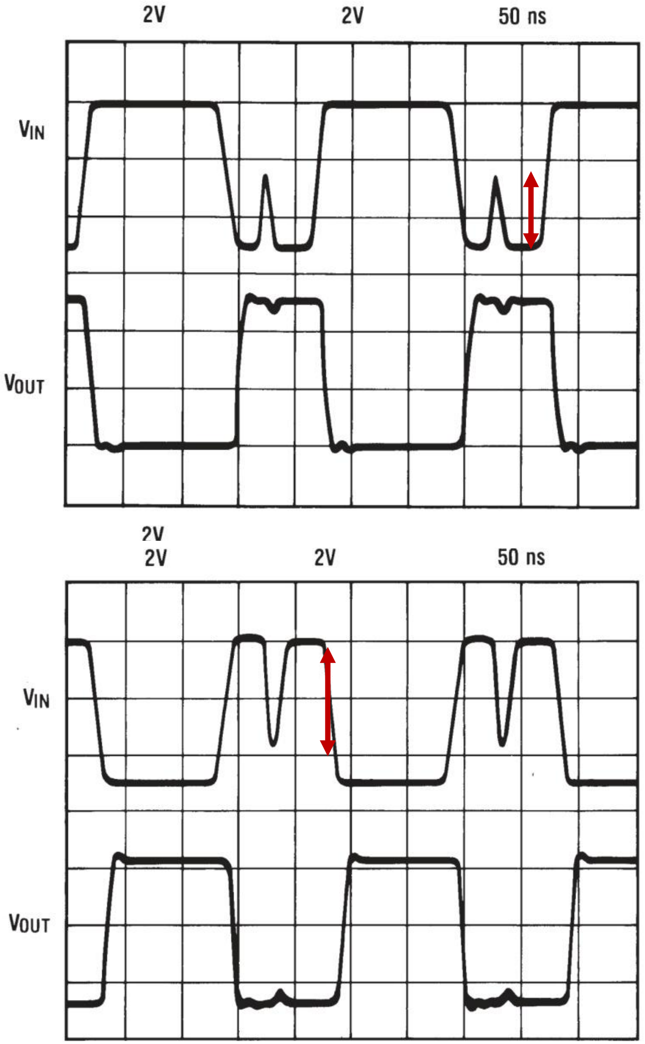
VNH = **0.1275 V** → Less than -8 dBm of power over 50 ohms!
VNL = **0.2325 V**

Noise Immunity

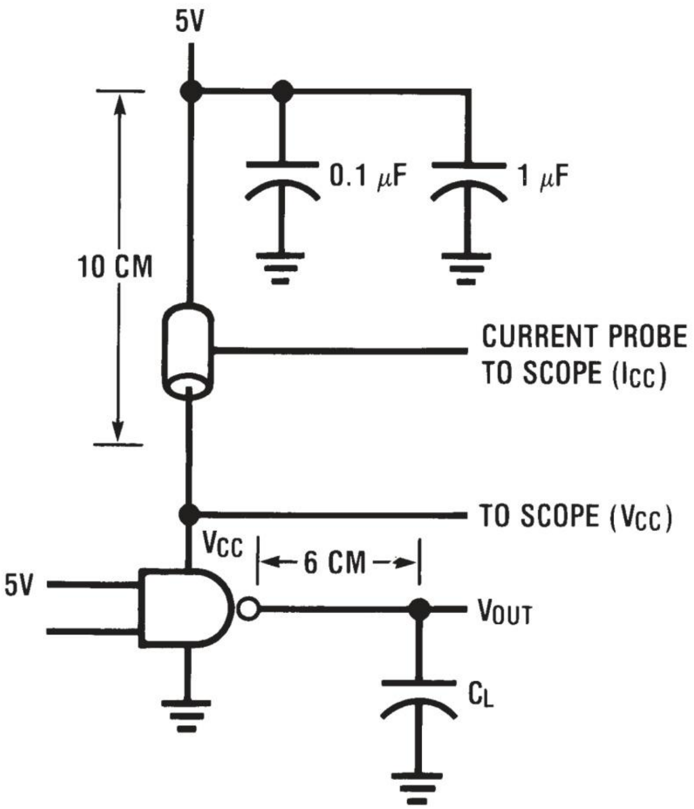


Response of a gate to noise spike, both positive and negative going.

Up to 2V immunity.

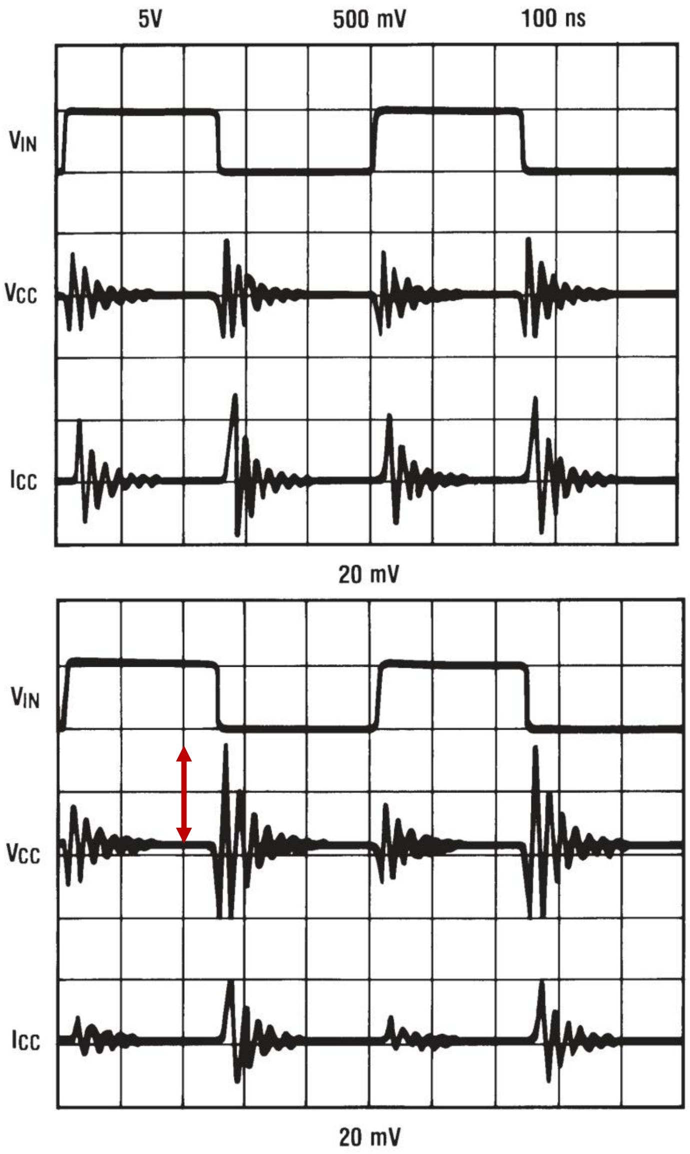


Noise Immunity



No load

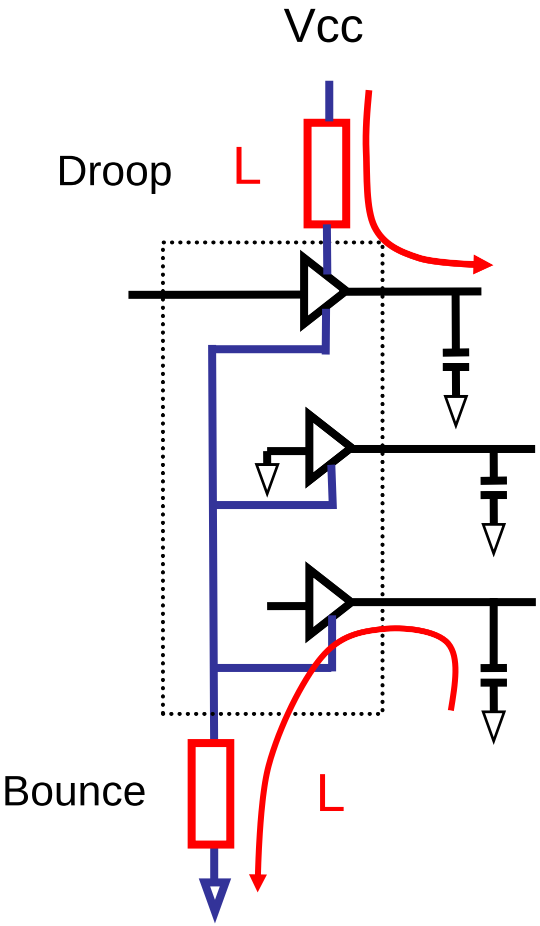
15 pf load



Effect of capacitive loads: With no load and with 15 pf

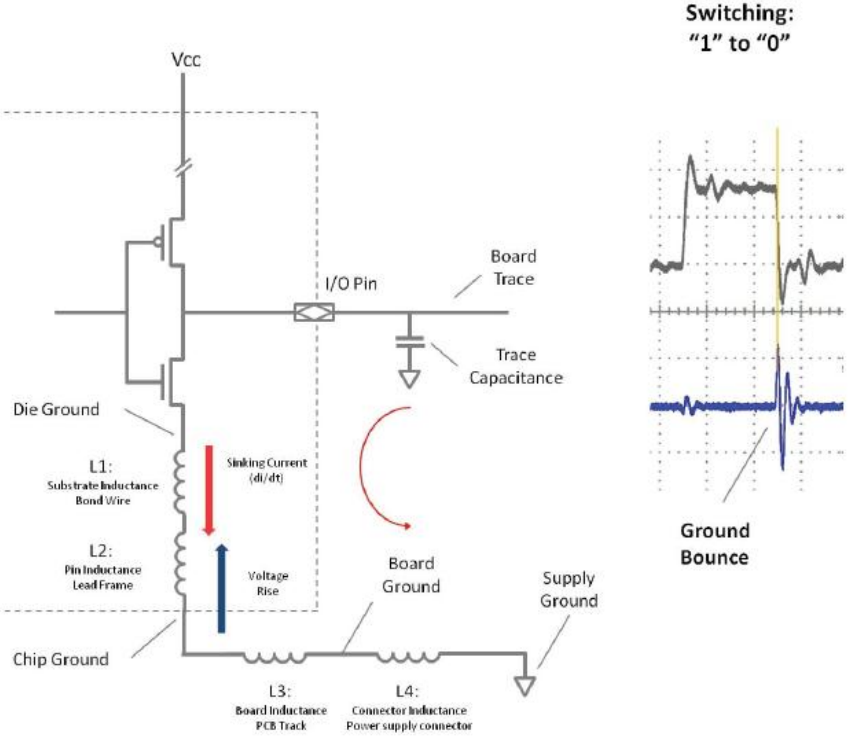
Digital Switching Noise

- Dynamic switching patterns in digital circuits
- Dynamic current drawn cause large temporal variation of voltage level
- Dynamic current can transform into noise by contributing voltage equal to **V =** **L_{sum}** × **(dI / dt)** across inherent inductances of device
- These noise are termed as Vcc Droop & Ground Bounce



Ground Bounce

- Ground path detailed between the power supply, board, device and output trace
- The path has four stray inductive sources from L1GND to L4GND that will sum together in series as Lsum
- V is the voltage difference between the die Vcc and ground caused by changing current through Lsum
- The voltage change with respect to time is equal to **$V = L_{sum} \times (dI / dt)$** across L1, L2, L3, and L4



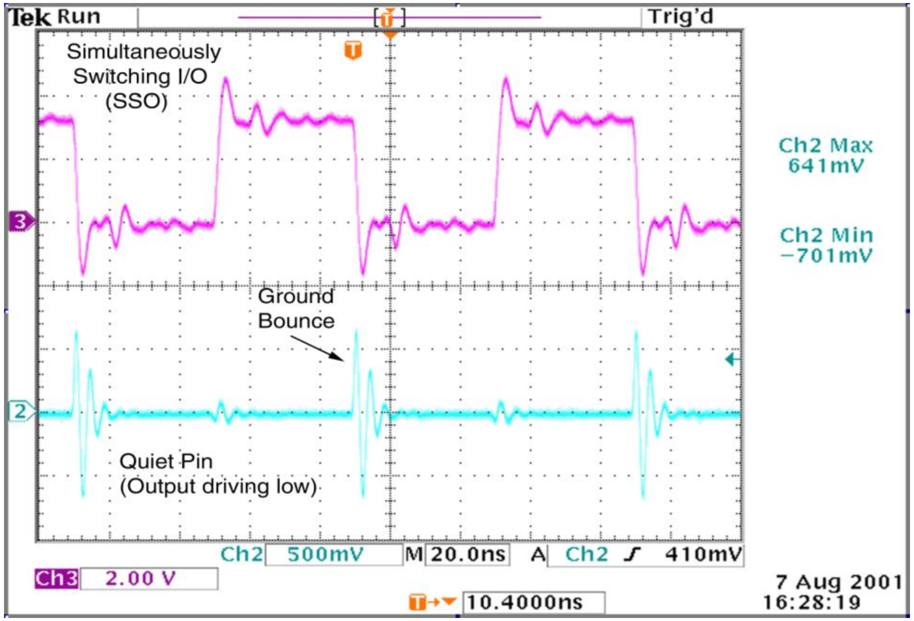
Ground Bounce Scope Example

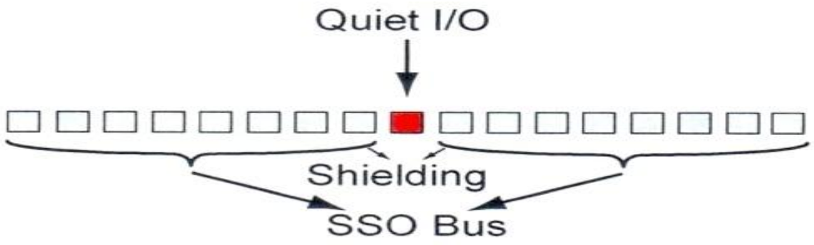
- CH3 - switching I/O pin

- CH2 - “quiet” I/O pin
  - Normally LOW
  - Resultant voltage change caused by changing current

- Ground bounces occurs with an output switch from logic level 1 to 0

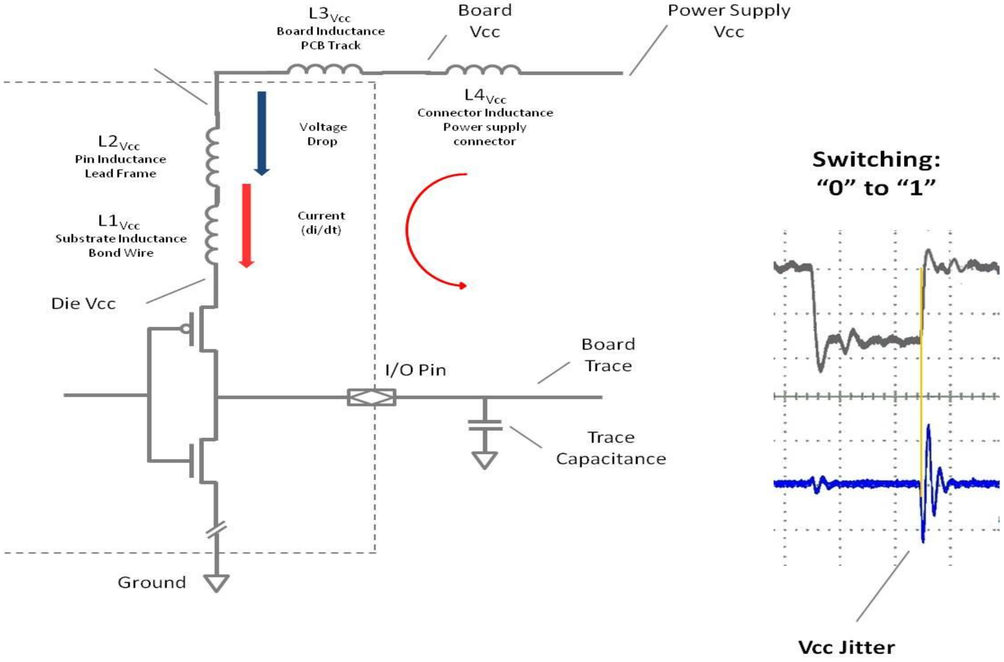
- High voltage ground bounce can be misinterpreted by the receiver as logic level 1 rather than 0





Vcc Droop

- Conversely, Vcc droop occurs when the output switches from logic level “0” to “1”
- Die Vcc level drops relative to the Power Supply Vcc.
- The power supply, board, device, and output trace capacitance are connected via the Hi-transistor
- The discharge current has to pass inductances L1Vcc to L4Vcc producing a voltage difference between the device die Vcc and power supply Vcc
- The voltage with respect to time, as with GND bounce, is **$V = L_{sum} \times (dI / dt)$**



Switch Mode Power Supply Noise

- Used on most modern electrical and electronic devices

- Very efficient compared to linear regulators and power supplies.

  SMPSs are very efficient compared to linear supplies, delivering power in response to a change in the output load and automatically adjusting to most world-wide power standards. The output power of SMPS is controlled using PWM (to drive high power transistors/FETs) with a lower duty cycle pulse delivering less energy to the output load

- Mechanism of generated noise

  The transistor switching speeds must be fast enough to control the energy transfer, can vary from 20 kHz up to several MHz and generate high-amplitude, high-frequency noise commonly known as switching noise.

- Limited resources to filter noise

  SMPS designers attempt to suppress this switching noise by using low pass filters (LPF) or bypass capacitors. However limited PCB space and cost can limit filtering capabilities hence noise can still be conducted and radiated into the surrounding circuits as EMI/RFI.

  Furthermore lower cost SMPSs may couple electrical switching noise back onto the main power line creating additional interference

EMI/RFI and Cross-talk Sources

- High EMI Oscillators

  All digital circuits require precise timing in the form of oscillators

  Oscillators can have high power at precise frequencies that radiate EMI/RFI

  The EMI/RFI can affect all adjacent circuitry

- High Speed Data Signals

  High frequency data signals with high power harmonic content radiate high frequency noise on to adjacent data paths or analog and RF transmission lines via cross-talk

  Depending upon the board layout, this high frequency noise can increase system BER, or show up as spurious signals if coupled on analog and RF lines.

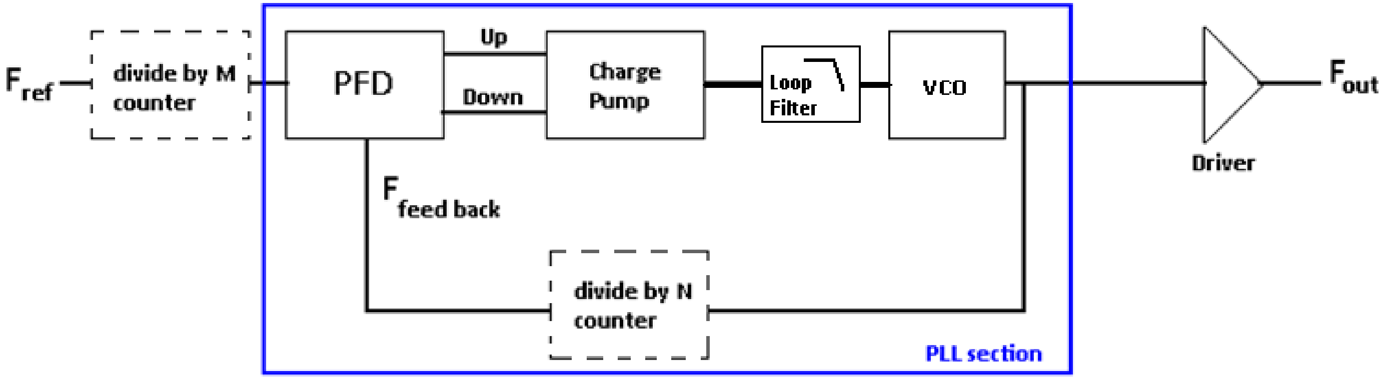
Highly Susceptible Devices

- Mixed signal environment
  - Sensitive analog IC's combined with noisy digital ICs
  - Handheld devices with radios
- High frequency PLL circuits
- High digital component count within a small footprint
- High I/O output pin counts within a small area
- Devices with lower power supply voltage requirements

Susceptible Devices

- Devices, ICs, Modules and PCBs:
  - PLL, Phase Lock Loop
  - Oscillators
  - FPGA
  - MMICs
  - ADC and DAC
  - Flash memory
  - Clock Distribution circuits
  - SerDes
  - 10-Gigabit Ethernet transceivers
  - All low-voltage devices

Example PLL Block Diagram



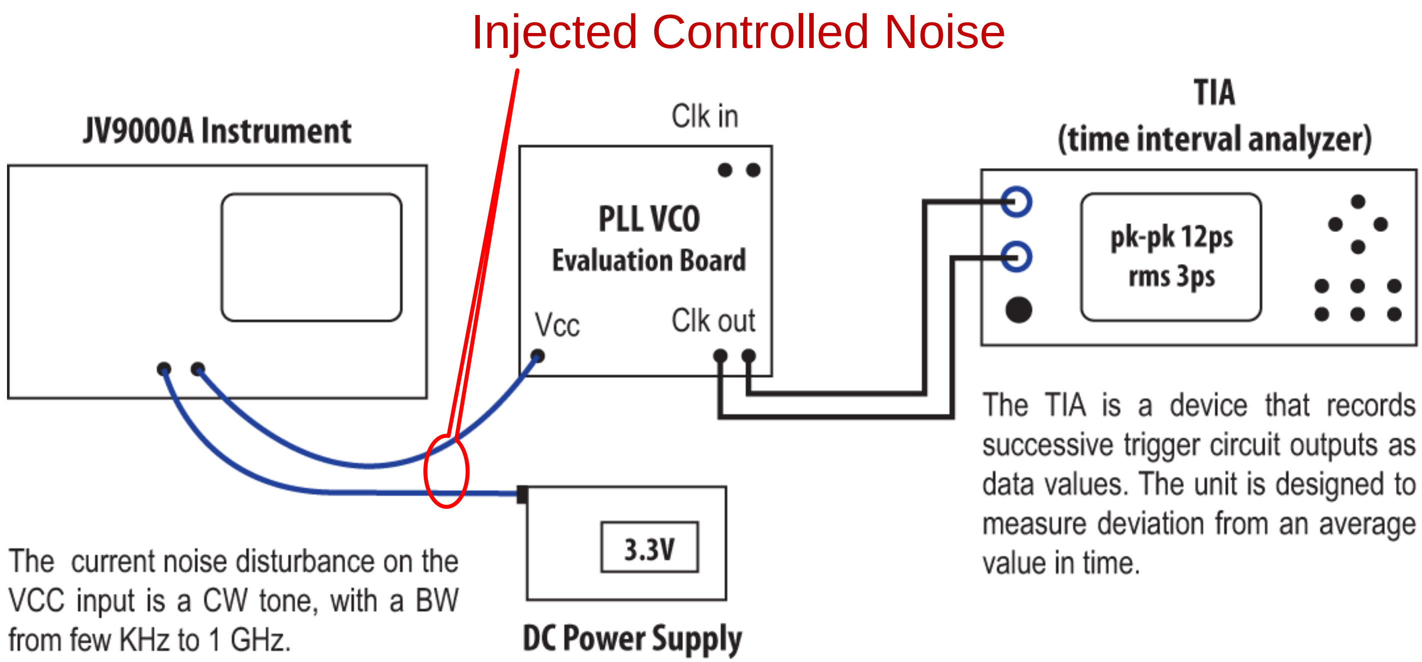
PFD - Phase Frequency Detector
VCO - Voltage Controlled Oscillator
M - optional pre-scale counter
N - optional feedback counter

- A closed loop system that generates a frequency-locked output (Fout) and corrects any phase shift by comparison to an input reference clock (Fref) via the feedback loop (Ffeedback)
- Major components are the Phase Frequency Detector (PFD), Charge pump, loop filter, VCO, pre-scale and feedback counters
- Uses master clock crystal/oscillator reference to lock phase with other clocks in the same system

Effects of Noise on PLL Circuits

- PLLs are widely used for generating high-precision, low jitter timing signals
- Their performance is highly susceptible to noise and interference
- PLL Noise
  - Power and ground plane noise that change the absolute reference values
  - EMI/RFI interference that penetrates the loop filter, VCO section of the PLL
  - Intrinsic jitter/noise from the reference oscillator
- Noise Effects
  - Noise on the circuit traces can cause the PFD to misinterpret the correct phase
  - Reference oscillator noise causes the PFD low/high outputs to constantly vary attempting to lock the phase
  - EMI/RFI on the loop filter, VCO network creates hysteresis in the PLL final output
  - The loss or the inability to lock the phase of Ref in and VCO output signal

Example PLL Test System

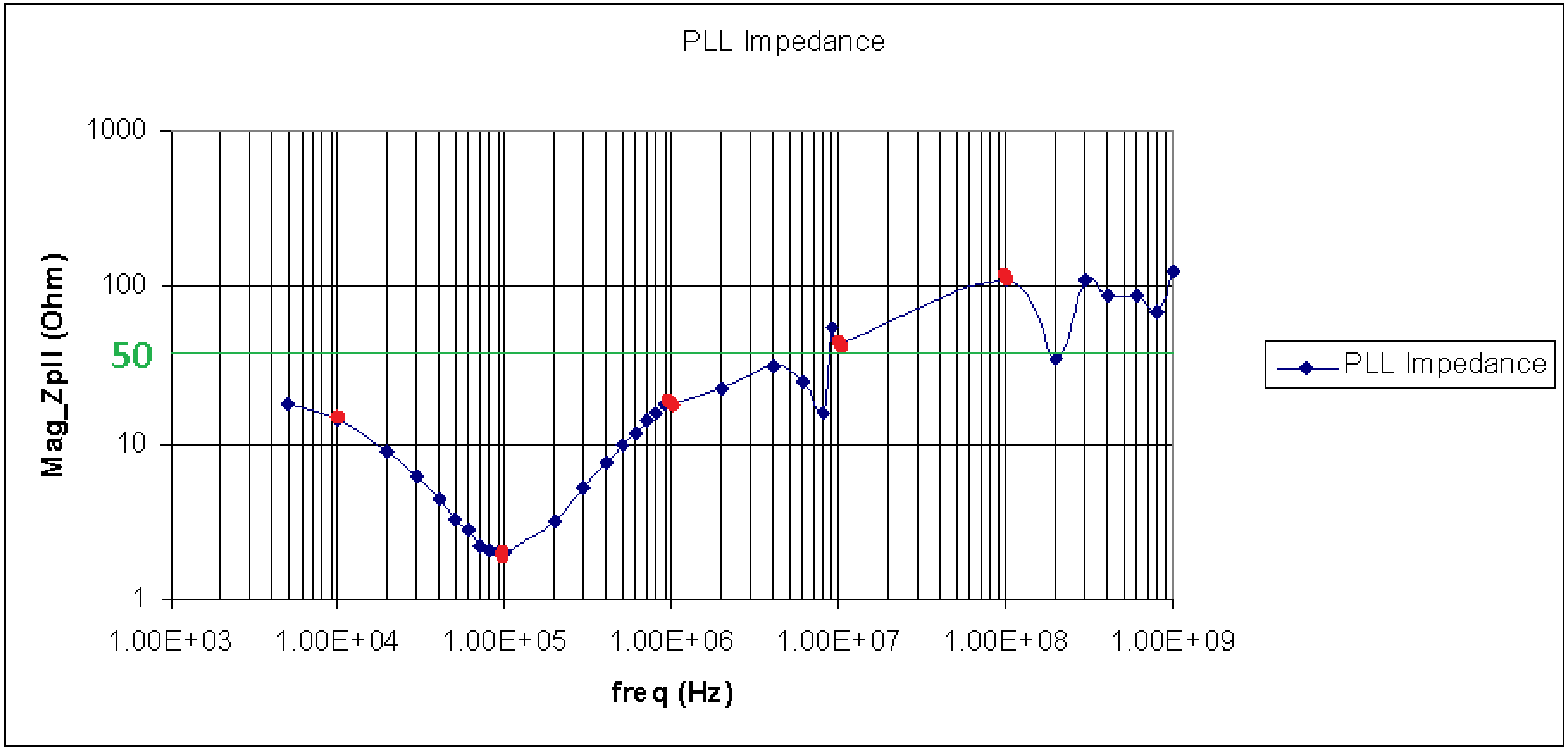

Injected Controlled Noise

The current noise disturbance on the VCC input is a CW tone, with a BW from few KHz to 1 GHz.

The TIA is a device that records successive trigger circuit outputs as data values. The unit is designed to measure deviation from an average value in time.

- Typical test system includes JV9000A noise generator, PLL evaluation board, DC power supply, and TIA (time interval analyzer) receiver
- An oscilloscope can be used in place of the TIA as the reference receiver
- One can also monitor phase noise

PLL Resonant Frequency Testing



Important frequency points

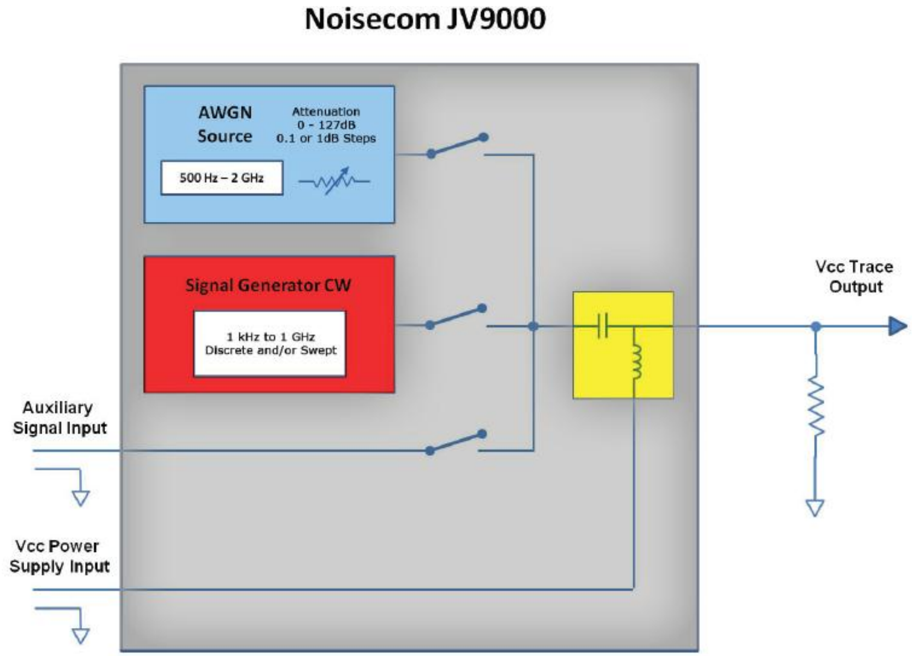
10KHz 100KHz 1MHz 10MHz 100MHz

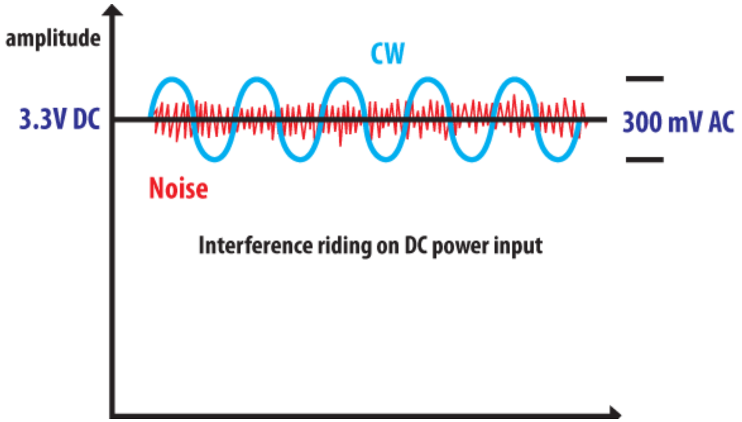
Standard Noisecom JV9000

- White Gaussian Noise Source
  - Noise Band: 500Hz to 2GHz
  - 500 mA, standard, higher current optional
  - Output Power: 0dBm into 50 ohms, attenuation range 0 to 127 dB with 0.1dB step size, higher output power optional
- Deterministic Jitter (optional CW spur generator)
  - Frequency range: 1KHz to 25MHz and/or 25 MHz to 3 GHz
- Ethernet, friendly GUI, NI Labview VIs

JV9000 Block Diagram

- AWGN, CW and auxiliary signals are combined with DC power via bias-Tee
- DC supply voltage powers the DUT through the JV9000 DC input
- Noise & CW signals disturb the DUT output





Interference riding on DC power input

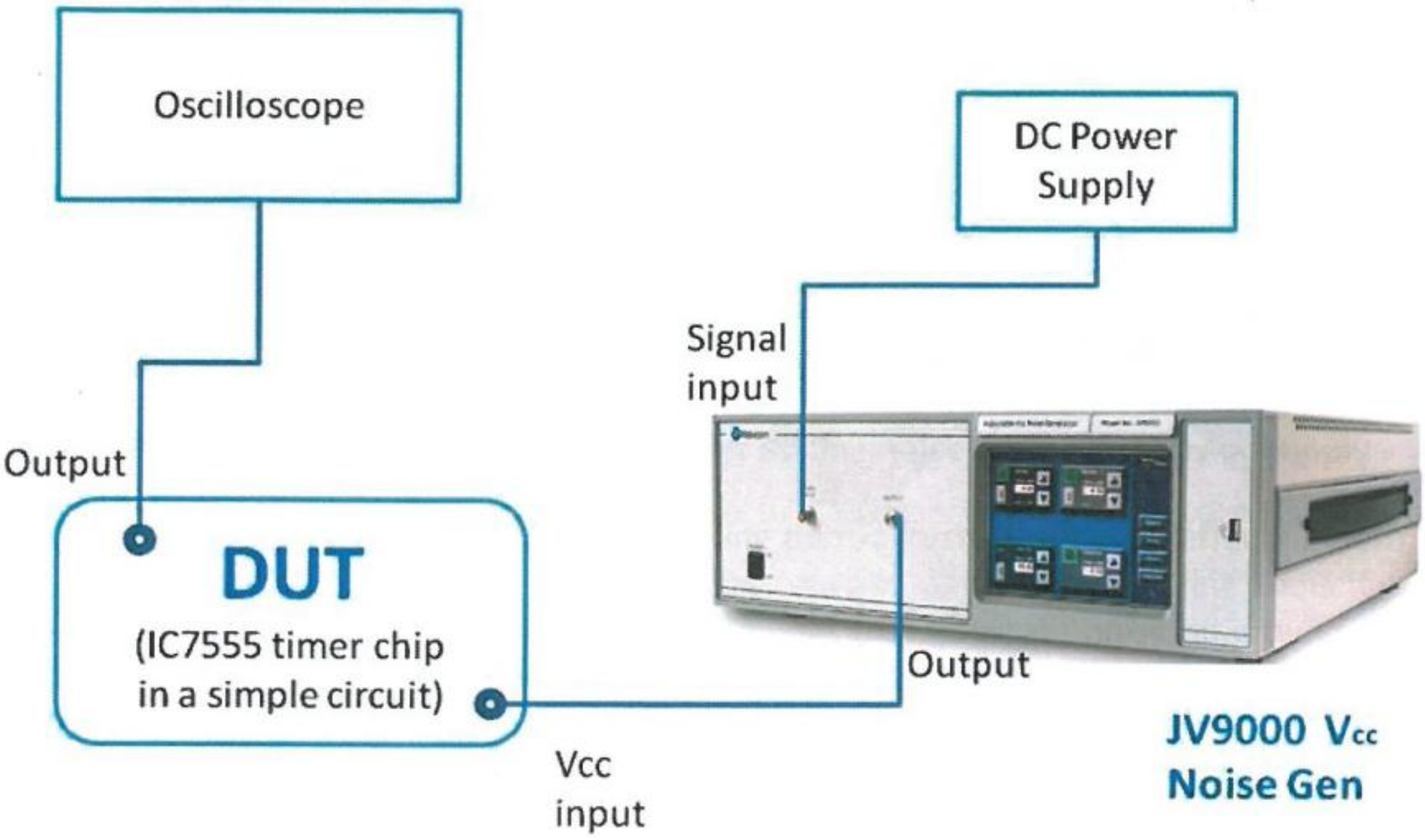
Options

- 10 dBm higher power noise/CW
- Higher frequency resolution, 1Hz
- Additional auxiliary inputs
- GPIB , 19” rack mount kit, auxiliary input(s)
- Higher current:
  - 2A, 50 kHz to 3 GHz
  - 5A, 10 MHz to 3 GHz
- 1 kHz-25 MHz or 25 MHz-3 GHz synthesizers
- Custom discrete sources, power levels & bands

JV9000 Noise on Vcc Applications

- Inject and simulate system noise
- Inject specific frequency for trouble shooting
- Testing PLLs
- Phase noise of crystal oscillators
- Test serial data converters
- Verify resonant frequency of the Vcc of the chip
- Noise tolerance of almost any chip

Noise on Vcc Test Demonstration



Oscilloscope

DC Power
Supply

Signal
input

Output

DUT

(IC7555 timer chip
in a simple circuit)

Output

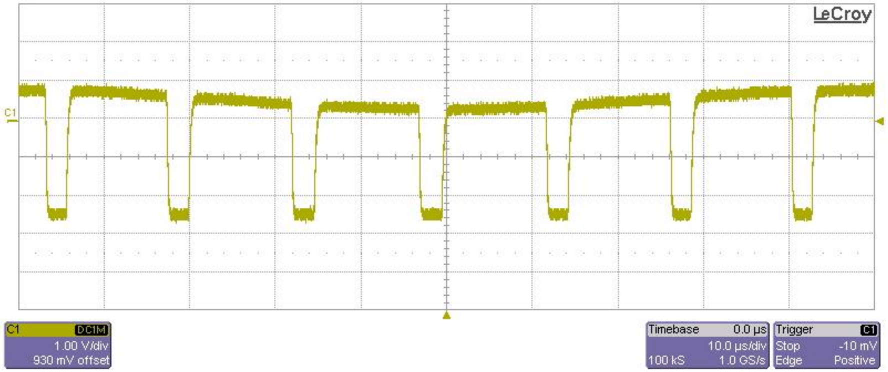
Vcc
input

**JV9000 Vcc
Noise Gen**

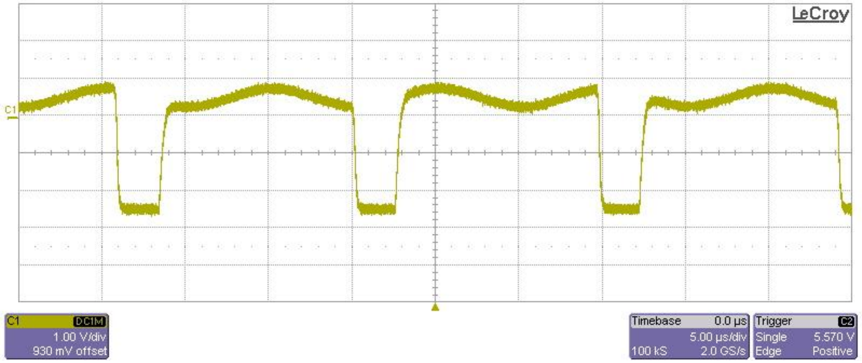
Block diagram of the “Noise on Vcc” test system

JV9000 Demonstration Results

- Top figure: 555 timer clock signal displayed on an oscilloscope
  - 10kHz CW is added to VCC



- Lower figure: 555 timer clock signal displayed on an oscilloscope
  - 100kHz CW is added to VCC



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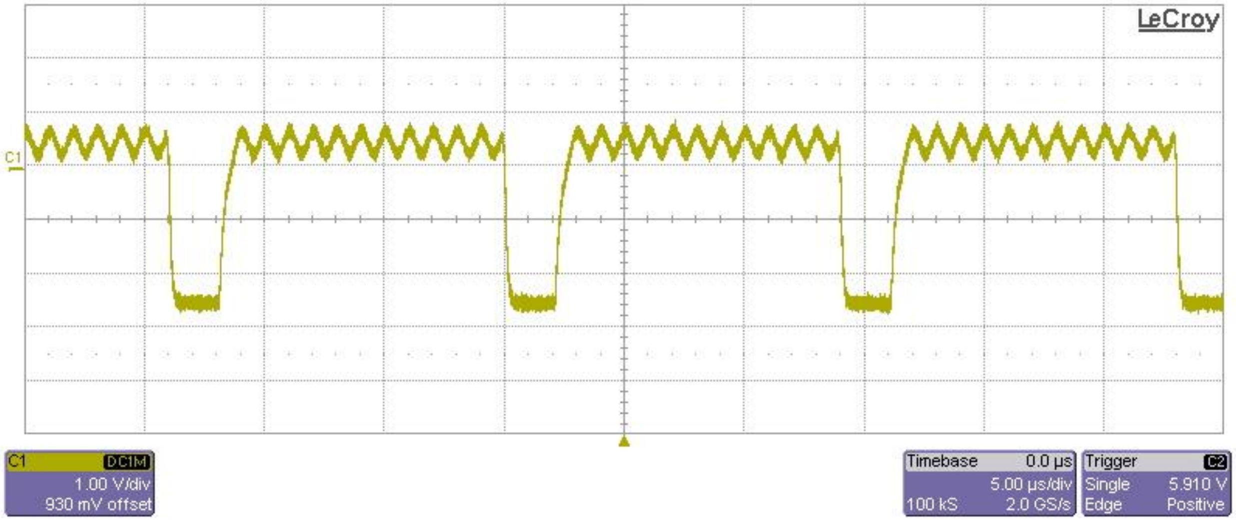
JV9000 Demonstration Results



- 555 timer clock signal displayed on an oscilloscope
  - 1 MHz CW is added to VCC

Summary

- All digital devices create noise
- RFIC mixed signal IC, high frequency PLL's and low voltage ICs are especially sensitive to noise
- These devices employ bypass capacitors, power & ground plane filtering, separate digital, analog power and ground planes attempting to eliminate noise
- Mixed signal RFIC's & HF PLL's are used in hand held devices with radios and microprocessors like smart phones, tablets, e-readers and notebook PC's
- These devices require sophisticated models and designs to improve noise immunity and need to be verified by testing
- The Noisecom JV9000A series can be used to test the accuracy of these software and hardware models and identify other immunity problems during engineering process, not after
- Broadband noise output
  - Used to measure the test system noise floor
  - Used to plot DUT input impedance vs. frequency

Noisecom Products

- <u>Noise Generating Instruments</u>
  - UFX Series Noise Generator
  - CNG-EbNo SNR Noise Generator
  - DNG7500 Digital Noise Generator
  - GPS7500 Noise & Interference Generator

- <u>Noise Generating Components</u>
  - Calibrated Sources
  - High Power Modules
  - Circuit Board Components
  - Diodes

- <u>Cryogenic Noise Standard</u>
  - NBS Series Primary Noise Standard

- <u>Various Additional Products by Application</u>
  - Noise figure
  - Satellite Channel Impairment
  - Jitter
  - Antenna Reference Sources
  - Basic Diode Circuit & Power Calculations

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Thank You for Participating in Today's Webinar

Any Questions?

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