SERDES Receiver Robustness and Bit Error Rate Testing Using the J7000B Noise Generator

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Abstract

High-speed Serializer/Deserializer (SERDES) is the backbone of modern digital communication systems used in Ethernet, PCIe, data storage, and high-speed digital interfaces. As the data rate increases to multi-GBPS, the reliability of the system is heavily dependent on noise, jitter, and signal integrity issues. Noise injection is a technique used to simulate real-world scenario and check the robustness of the system with reduced signal-to-noise ratios (SNR). In this application note, the use of a Maury Microwave J7000B broadband noise generator is presented in the context of SERDES testing, focusing on robustness of a SERDES receiver, bit error rate (BER) testing, and link margin testing.

High-Speed SERDES Receivers

Digital communication systems rely on high-speed serial links for chip-to-chip and board-to-board communication. Data rates commonly range from approximately 1 Gbps to tens of gigabits per second to meet performance requirements of modern systems. These high-speed links often use SERDES architectures to achieve the required data rates. For transmission, parallel data is serialized into a high-speed serial stream. The receiver then deserializes the serial stream back into parallel data. Common interfaces implemented with SERDES technology include Serial Gigabit Media Independent Interface (SGMII) for Ethernet networking; Peripheral Component Interconnect Express (PCIe), widely used for high-speed internal system interconnects; Serial ATA (SATA) for storage devices; and JESD204, commonly used in data converter and RF systems.

At these speeds, system performance is significantly impacted by the following sources of impairment:

- **Thermal Noise:** All electronic components generate random electrical noise due to the thermal motion of charge carriers. Commonly referred to as thermal noise, its power increases with temperature and contributes to the overall noise floor.
- **Crosstalk:** In serial data links, crosstalk occurs when signals from adjacent traces or channels couple together and interfere with one another.
- **Power Supply Noise:** Voltage fluctuations from the power supply can affect circuit operations.
- **Electromagnetic Interference (EMI):** Electromagnetic energy from external devices or systems can interfere and be coupled into a communication link.
- **Channel Loss and Reflections:** The communication signal is attenuated as it propagates through the transmission channel, while reflections result from impedance mismatches along the signal path.

Regardless of their source, these impairments reduce receiver margin and ultimately limit link performance. Injected noise causes amplitude degradation by reducing the effective SNR at the receiver, decreasing signal amplitude margin and reducing eye opening. Noise on the signal path can also affect clock and data recovery circuits of the SERDES system, increasing timing uncertainty. Both amplitude degradation and timing uncertainty are reflected in the measured BER, which indicates the number of incorrectly received bits compared to the total number of transmitted bits. BER testing provides insight into receiver robustness and sensitivity, as well as available link margin.

Noise Generator-Based SERDES Receiver Testing

To ensure the reliable operation of a SERDES system, the receiver should be tested under varying SNR conditions. Precision noise generators, such as the Maury J7000B Jitter Noise Generator, can combine broadband additive white Gaussian noise (AWGN) with a digital signal to test the robustness of a SERDES receiver.

J7000B Series Noise Generator-Based Testing Benefits

The Maury J7000B generates AWGN with a large crest factor to model real-world random jitter (Rj) in high-speed serial links. By injecting precise amounts of noise into a data stream, engineers can evaluate receiver performance, characterize SNR degradation, and determine receiver margin. The J7000B supports qualification and characterization of both single-ended and differential serial devices and can be configured to satisfy a wide range of test requirements.

Key benefits of J7000B-based SERDES receiver testing include:

- **Controlled Stress Testing:** Enables accurate replication of real-world noise conditions in a controlled laboratory environment, allowing receiver performance to be evaluated under degraded signal conditions.
- **Repeatability:** Provides consistent and repeatable test conditions across multiple devices and test runs, improving confidence in measurement results.
- **Receiver Margin Characterization:** Helps quantify receiver tolerance to noise and identify performance limits before the receiver fails to meet BER requirements.
- **Adaptable Design:** The unit can be configured with many options to satisfy specific test system requirements.

Noise generator-based SERDES testing is widely used across a variety of industries and applications to evaluate receiver robustness, signal integrity, and overall link performance under realistic operating conditions. Common applications include semiconductor device validation, network equipment testing, characterization of high-speed interfaces, validation of data center hardware, and aerospace and defense digital communication systems.

SERDES Noise Injection Test Configuration

A SERDES noise injection test configuration is shown in Figure 1. In this setup, a known data pattern is generated and combined with controlled broadband noise before being applied to the SERDES receiver. By varying the injected noise level and monitoring receiver performance, engineers can measure BER and evaluate receiver sensitivity.

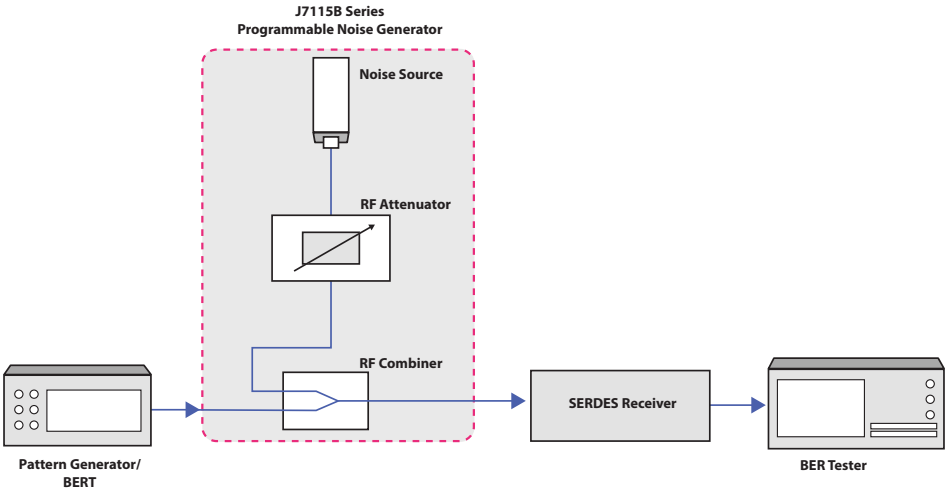


Figure 1. A SERDES noise injection test configuration using the Maury J7115B Jitter Noise Generator.

The main components of the test system include:

- **PRBS Generator:** Generates a pseudo-random bit sequence (PRBS) that serves as a repeatable test signal for stressing the SERDES receiver.
- **Noise Generator:** Injects controlled broadband noise into the signal path to emulate degraded operating conditions.
- **Power Combiner:** Combines noise with the digital signal.
- **Variable Attenuator:** Changes the level of additive noise on the signal.
- **BER Tester:** Measures the bit error rate.

By gradually increasing the injected noise level and monitoring BER, the receiver's noise tolerance and performance limits can be quantified in a controlled and repeatable manner.

Example Application of SGMII SERDES Testing

The SGMII is a commonly used high-speed serial interface in networking equipment. The following example illustrates how controlled noise injection can be used to evaluate receiver sensitivity and BER performance in an SGMII SERDES link. Typical characteristics include a data rate of 1 Gbps, and up to 2.5 Gbps in certain implementations.

A typical test procedure consists of the following steps:

- **Step 1:** Generate a PRBS using a pattern generator.
- **Step 2:** Set the transmitter to its nominal output amplitude.
- **Step 3:** Use a J7115B Noise Generator to introduce controlled broadband noise into the signal path.
- **Step 4:** Gradually increase the injected noise level while monitoring receiver performance.
- **Step 5:** Measure and record BER as a function of the injected noise level.

By observing the noise level at which BER begins to increase significantly, engineers can characterize receiver sensitivity and determine the available link margin. Typically, the receiver sensitivity limit is defined by the noise threshold at which BER exceeds 10^{-12}.

Important SERDES Noise Testing Measurements

Receiver performance is commonly evaluated using measurements that quantify the effects of injected noise on signal integrity and timing margin. Among the most widely used are eye diagrams and bathtub curves.

Eye Diagram

An eye diagram is used to show the signal integrity of a digital link. The eye-shape pattern of the graph is formed by overlaying multiple bit periods over one another. Figure 2 highlights a few key areas of the diagram. The eye opening in the center indicates the receiver's ability to distinguish between logic states and its size is commonly evaluated using eye height and eye width. Eye height represents the voltage margin, or the separation between logic states, while the eye width represents the timing margin for the receiver to sample bits correctly.

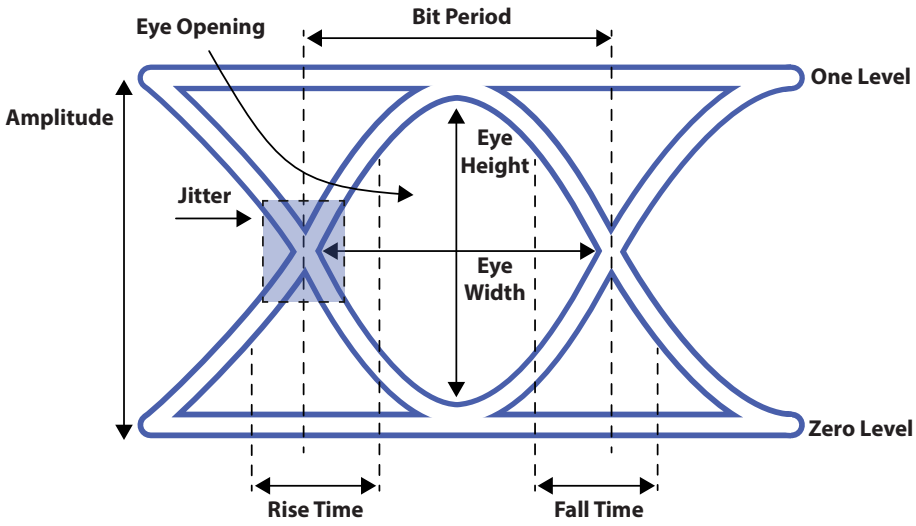


Figure 2. An eye diagram highlighting key characteristics used to evaluate the signal integrity of a digital link.

Introducing noise into the signal path directly impacts eye diagram characteristics. Eye height reduces with random voltage noise, while eye width reduces with increased random jitter. These effects cause the eye opening to become smaller, reducing the receiver's decision margin. As the eye closes, the probability of incorrect bit decisions increases, resulting in a higher BER. Eye diagrams are typically measured using high-bandwidth oscilloscopes to evaluate signal integrity and monitor these effects under varying operating conditions.

Bathtub Curve

A bathtub curve (Figure 3) provides a statistical view of the eye diagram. It plots BER as a function of sampling position across the eye opening. BER is lowest near the center of the eye, which has the largest timing margin, and increases as the sampling position approaches the left or right edge of the eye.

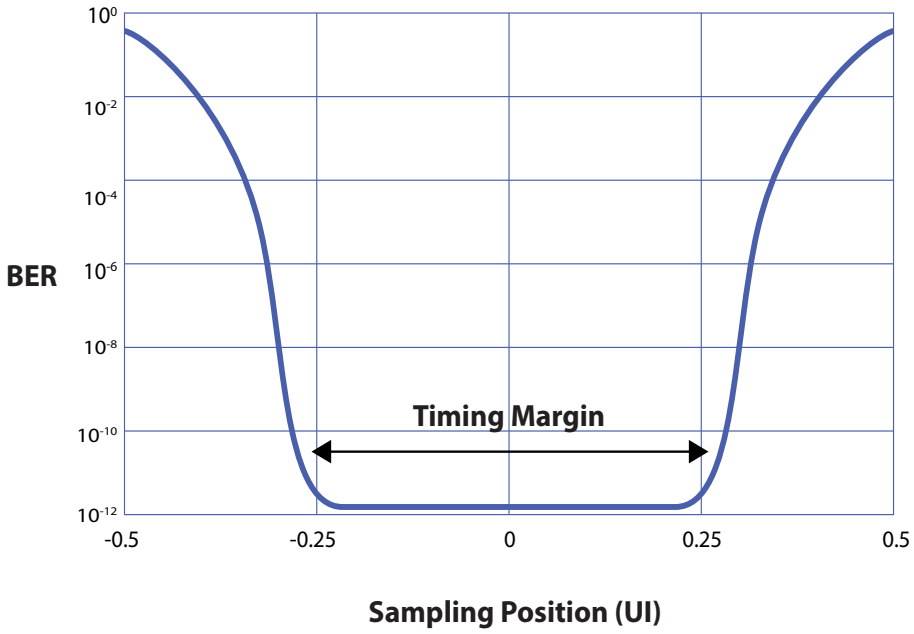
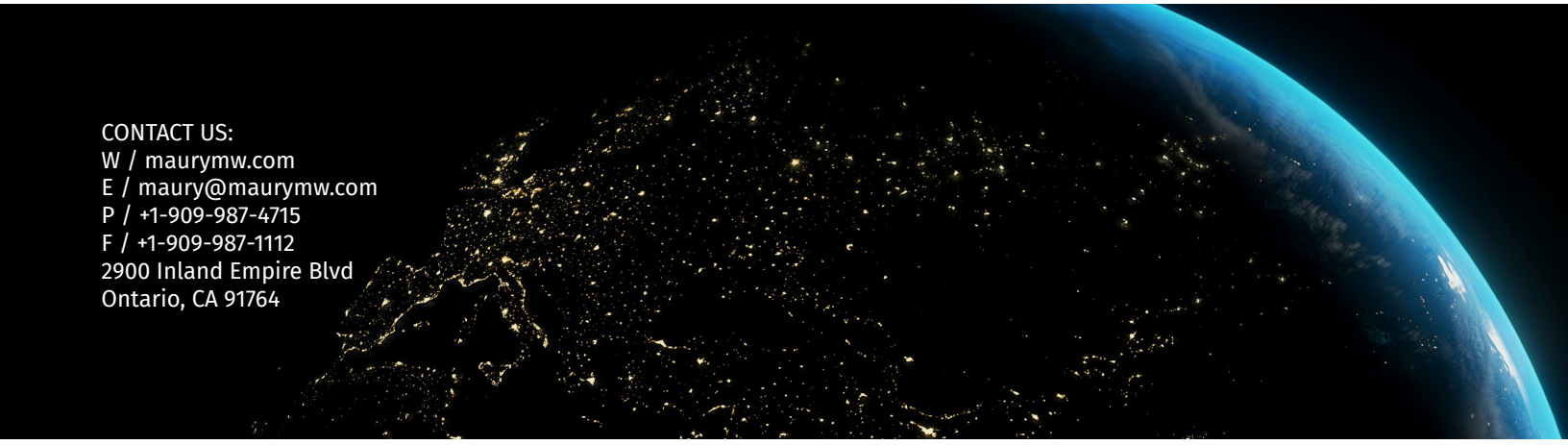


Figure 3. Bathtub curve showing BER vs the sampling position across the eye opening.

SERDES Receiver Testing with Controlled Noise Injection

As SERDES data rates continue to increase, maintaining reliable receiver performance under degraded signal conditions becomes increasingly important. Controlled AWGN generation with the J7000B provides a repeatable method for characterizing receiver sensitivity, evaluating BER performance, and determining available link margin. Combined with eye diagram and bathtub curve analysis, these measurements provide valuable insight into signal integrity and SERDES receiver robustness.



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